A Manycore Coprocessor Architecture for Heterogeneous Computing

Andreas Olofsson
Adapteva Inc

Over the last two decades we have seen amazing strides in raw computing performance in stationary as well as portable systems. Unfortunately, advancements in processing efficiency have come at a slower pace. Without significant improvements in energy efficiency, advances in high performance computing systems will soon stall. As an industry we are now faced with a tough choice. Do we continue using general purpose processors for high performance computing and accept the fact that year over year performance improvement will slow down and or do we look for a new approach with significantly better energy efficiency but which may be harder to use? In this talk, I will present some possible paths forward and propose a heterogeneous computing architecture with an order of magnitude improvement in power efficiency. The proposed architecture leverages the strengths of FPGA, microprocessor, and coprocessor technology to simultaneously offer great processing efficiency and a familiar programming model.

Biography:
Andreas Olofsson has over ten years of experience in the specification and design of Digital Signal Processors, microcontrollers,and mixed signal chips at Analog Devices and Texas Instruments and has completed over twenty tapeouts in process technologies from 0.35um to 65nm. From 1998-2006, Andreas was a design leader in the development of the TigerSHARC DSP family, a revolutionary new computer architecture which at the time of release was the world leader in floating point energy performance with an efficiency of 0.75GFLOPS/Watt in a 0.13um process. He is currently the president of Adapteva Inc, a fabless semiconductor company with a mission to drastically improve power efficiency in high performance computing applications. Andreas received his BSEE, BS in Physics, and MSEE from the University of Pennsylvania.