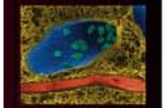
Laboratory Directed Research and Development - Postdoctoral Research and Development

**LDRD DAY**

**A Look Into the Future of Los Alamos**

# Novel Semiconductor Nanowire Architectures

Shadi A. Dayeh, Postdoc



**Innovation for Our Nation**

## What makes this research exciting?

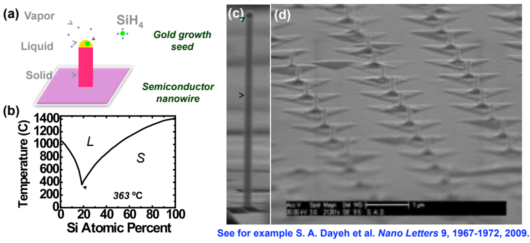
- To meet national and global future energy needs, the efficiency of converting solar energy to electrical energy needs to be enhanced, and the cost of manufacturing such highly efficient solar cells needs to be reduced.
- Concurrently, device miniaturization have allowed the realization of high-speed electronic devices, however with large standby power dissipation, not to mention physical limits imposed on further device scaling.
- We propose utilizing the 1D nature of semiconductor nanowires for efficient solar cells, low-power and high-speed electronics, and bio-interfacing.

### *What are semiconductor nanowires?*

Semiconductor nanowires are 1D nanostructures with unusual optical and electronic properties. Some of their characteristics include:

- Quantum confinement in 2D.
- Material and device engineering in 3D, and flexibility in heterostructuring (i.e. combining different materials with different characteristics).
- Small geometry for dense device integration.
- Single crystal with high quality that can be grown at lower temperatures and costs than typical semiconductors.

### *How do nanowires grow?* By the vapor-liquid-solid (VLS) mechanism:



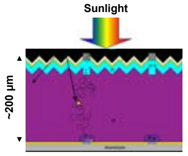
See for example S. A. Dayeh et al. *Nano Letters* 9, 1967-1972, 2009.

(a) Cartoon illustrating the VLS growth mechanism. Input materials from the vapor ($SiH_4$) decompose on the liquid Au nanoparticle surface and diffuse to precipitate at the liquid-solid interface in the form of a solid wire and thus the name VLS mechanism. (b) Au-Si phase diagram: The VLS growth occurs in the vicinity of the Au-Si eutectic temperature (~ 363 ºC). (c) ~ 88º angle view scanning electron microscope (SEM) image of a vertical semiconductor nanowire on a growth substrate. (d) ~ 83º angle view SEM image of an ordered array of vertical semiconductor nanowires on a growth substrate. Ordering nanowires in a specific pattern is useful for functional nanoscale systems.

## What is the approach?

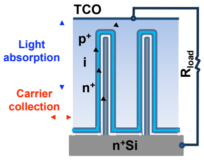
- **Solar cells:** Align nanowires end-on to the sun so that light is absorbed along their length, while electrons easily escape to the side.

**Conventional planar solar cell**



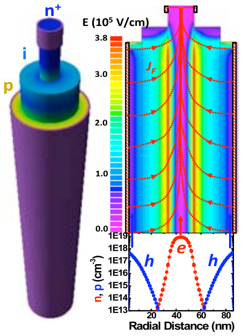
Incident light energy is converted to charge carriers that have to diffuse few hundred microns to reach contact electrodes; they recombine before reaching the electrode and cell efficiency drops.

**Radial nanowire solar cell**



Light absorption occurs in the vertical direction, and carriers can be quickly drifted in the lateral direction, ideally with no recombination leading to higher cell efficiency.

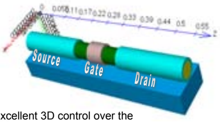
**Field distribution and carrier separation in a nanowire solar cell**



In a radial nanowire p-i-n junction, material doping and composition can be easily tuned. Left: A core/shell n-i-p nanowire used in our simulations. Right: The built-in electric field extends throughout the nanowire structure such that charge carriers can be separated fast over short distances and collected at correspondent electrodes.

- **Electronics:** Utilize flexibility in axial and radial material composition to design transistors that can operate at high-speed, at low-power, and with less standby power dissipation.

**Nanowire Transistor**



Excellent 3D control over the channel electrostatics

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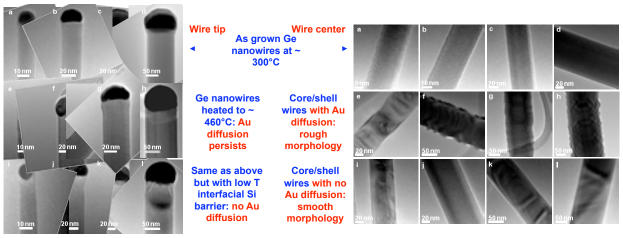
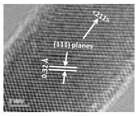
## What have we learned so far?

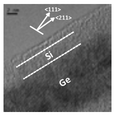
**Radial nanowire heterostructures:**

- Growth of Ge nanowires at low temperature (~ 300°C) and Si shells at higher temperature (~ 600°C) lead to gold diffusion, which causes bad nanowire morphology and bad transport characteristics.
- Previous work did not solve this problem.
- We were able to grow core/shell Ge/Ge and Ge/Si without gold diffusion by engineering the nanoparticle interface.





High Resolution Transmission Electron Microscope (TEM) image of a single crystal 10 nm diameter Ge nanowire where lattice fringes of atomic planes are clearly seen.

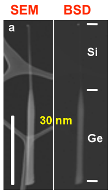


High Resolution TEM image showing 2nm single crystal Si shell deposited on the 10 nm diameter Ge wire. With the growth technique we developed, we are able to grow such heterostructures with no detrimental Au diffusion.

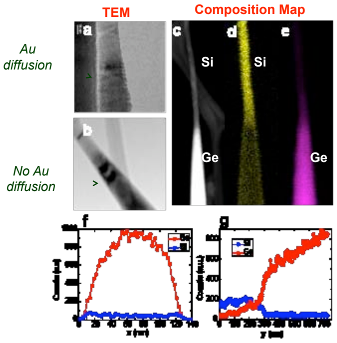
→ Bandgap engineered Tandem solar cells, heterostructure transistors, Infrared detectors, etc.

**Axial nanowire heterostructures:**

- Previous work realized a maximum of ~ 20% axial composition modulation and did not solve the gold diffusion problem at the interface.
- By maintaining high precursor partial pressures and proper tuning of the rate and time of temperature switching, we were able to grow high-quality 100% composition modulated nanowires.



SEM and Back-scattering detector images of an axial Ge → Si nanowire heterostructure. These wires are excellent candidates for next generation tunnel transistors.



TEM images at the junction of the Ge/Si nanowire heterostructure (a) with Au diffusion, and (b) with our new growth procedure and no Au diffusion. (c) STEM image at the junction showing bright Ge and dark Si segments. (d) – (e) False color contour maps showing (d) Si content and (e) Ge content. (f) Energy dispersive x-ray (EDX) line spectrum across the radial direction of the Ge segment showing no Si shell coating. (g) EDX line spectrum in the axial direction, at the junction, showing transition from pure Ge to pure Si. A transition segment of diffusive SiGe interface is observed with a length of ~ 200 nm. This allows band-engineering in the direction of charge carrier flow, which is exclusively provided by this system.

## Why is this important for our nation?

Demonstration of such aggressive modulation in material synthesis, uniquely achieved at LANL allows:

- Reduction of cost in solar cell manufacturing from 0.276 $/KWh for bulk single-crystal Si, to 0.162 $/KWh for radial Si nanowire cell (assuming only 15 % efficiency).
- Possibility of enhancing the quantum efficiency to 100 % leading to an overall cell efficiency of ~ 28 %, higher than 24.5 % record efficiency for high-cost bulk Si cells.
- Superior speed and multi-functionality for future electronic systems with less heating and low standby power, all at low cost.

## About the Postdoc

Dr. Shadi Dayeh

Dr. Shadi Dayeh is a Director's Postdoctoral Fellow in the Material Physics and Applications Division with the Center of Integrated Nanotechnologies. He works on this LDRD project under the mentorship of **Principal Investigator Samuel Picraux**.

Dr. Dayeh earned his Maitrise-en-Sciences from the Lebanese University in Physics/ Electronics in 2001, MS in Electrical Engineering from Southern Methodist University in 2003, and Ph.D. in Electrical Engineering (Applied Physics) from UC San Diego in 2008.

His research interests include growth, characterization, device physics and fabrication, and the integration of III-V and Si/Ge semiconductor nanowires. Dr. Dayeh is the winner of 5 best paper awards for his PhD work, and is currently the IEEE Electron Device Society Ambassador/Lecturer for the America North West region.

**Goals for the future:** Become a faculty member in the US to continue his research and learning, and contribute to the education of future scientists and engineers.