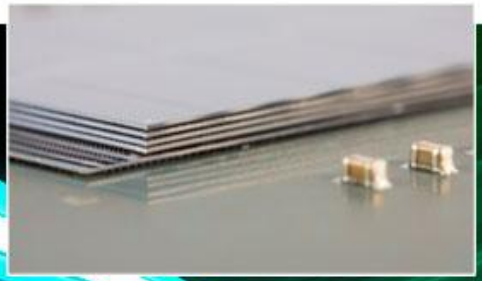
HMC YOUR NEW STANDARD FOR MEMORY PERFORMANCE



Todd Farrell

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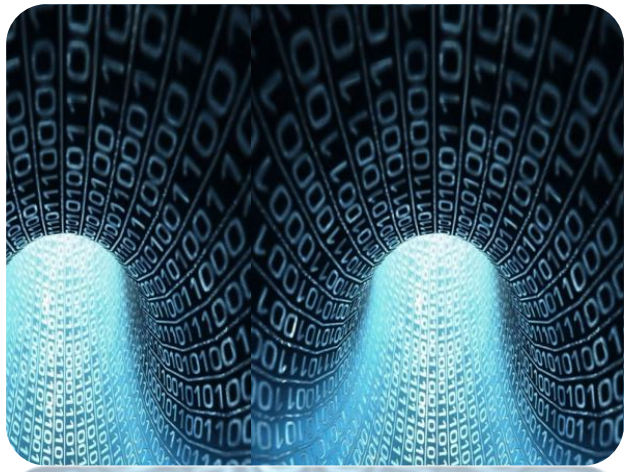
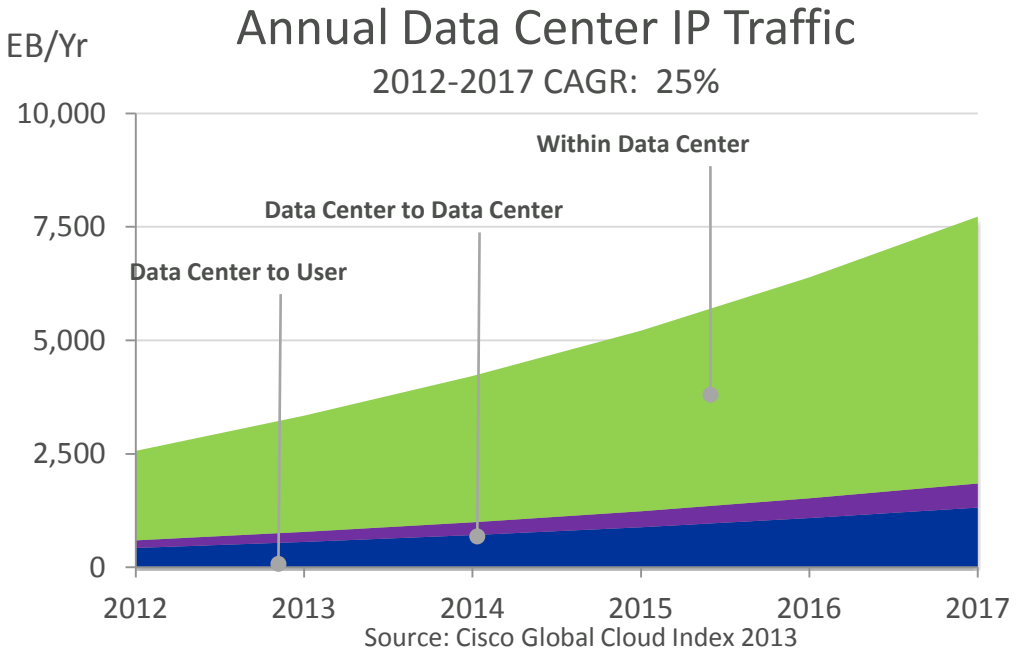
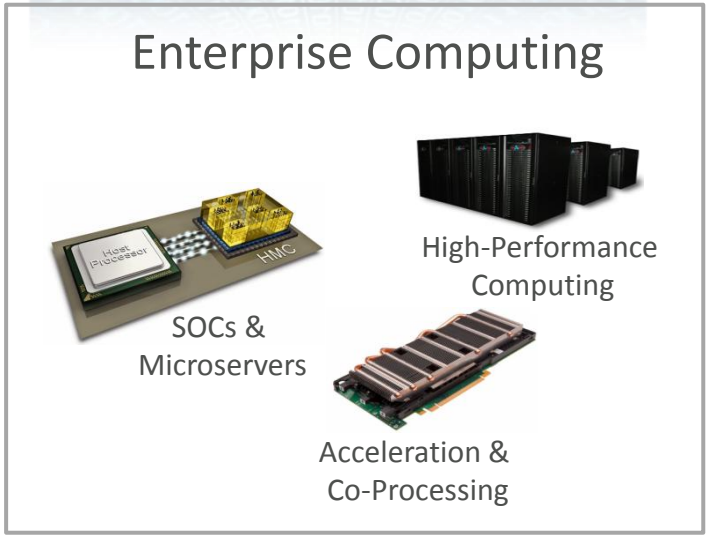
Demand Drivers

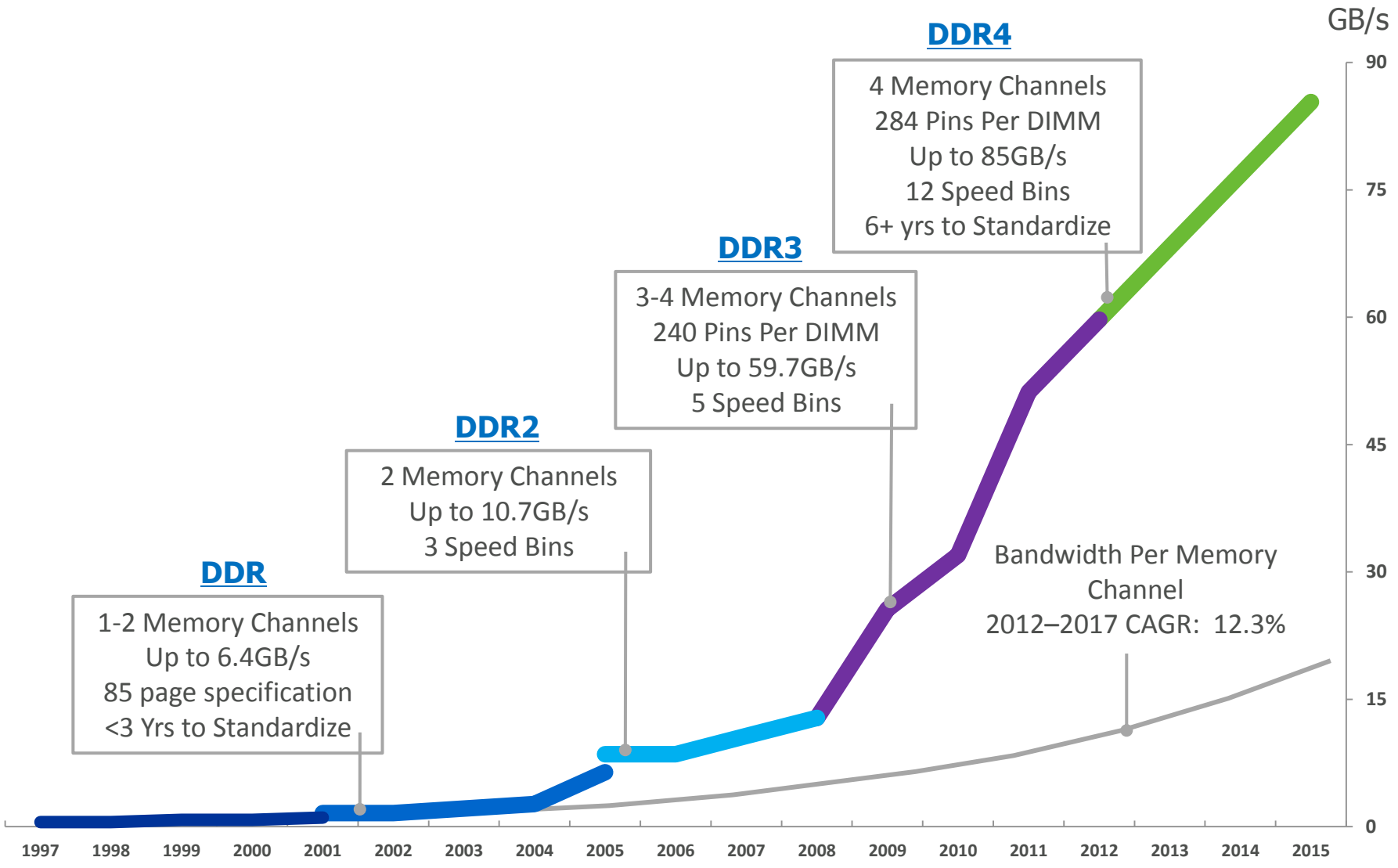
- Insatiable need for bandwidth
- Impact of the cloud
- Global demand for mobility
- Big data analytics challenge







Historical System Bandwidth, Cost, and Complexity



Traditional Memory Designs Do Not Scale and Drive Exponential Complexity

Major Challenges to the Longevity of DRAM and NAND Technologies

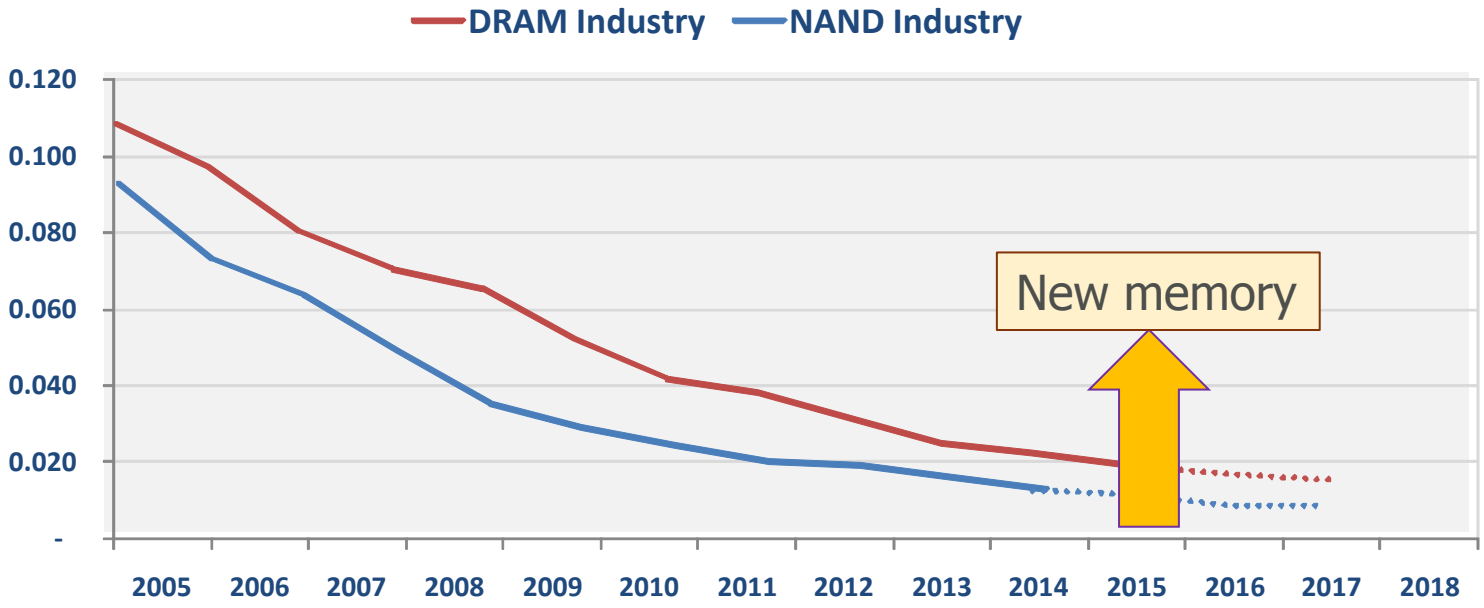
Endurance
- Cycling capabilities

Shrink
- Physical limitations

Equipment capability
- Increasing equipment complexity

Cost
- Path of diminishing returns

Memory Process Nodes Over Time



HMC - A Revolutionary Shift

Increased Bandwidth

Greater Power Efficiency

Lower TCO

Reduced System Latency

Smaller, Scalable and Flexible

MICRON HMC

High-Performance Memory Comparison

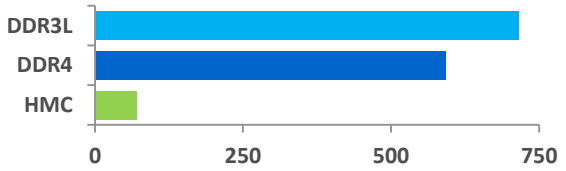
Single-Link HMC vs. DDR3L-1600 and DDR4-2133
What does it take to support 60 GB/s?

Requirements

TCO Valuation

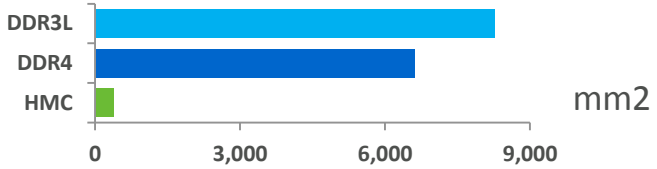
Channel Complexity

90% simpler than DDR3L
88% simpler than DDR4



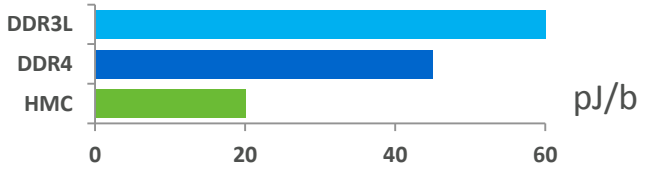
Board Footprint

95% smaller than DDR3L
94% smaller than DDR4



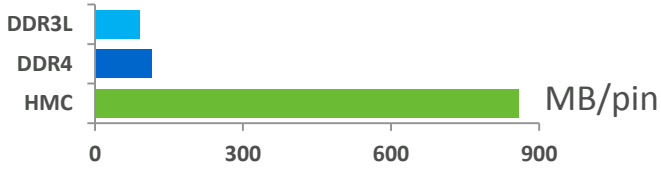
Energy Efficiency

66% greener than DDR3L
55% greener than DDR4



Bandwidth

10.2X greater than DDR3L
8.5X greater than DDR4



Enabling Technologies

Abstracted Memory Management

Memory Vaults vs. DRAM Arrays

- Significantly improves bandwidth, quality, and reliability vs. traditional DRAM technologies

Logic Base Controller

- Reduces memory complexity and significantly increases performance
- Allows memory to scale with CPU performance

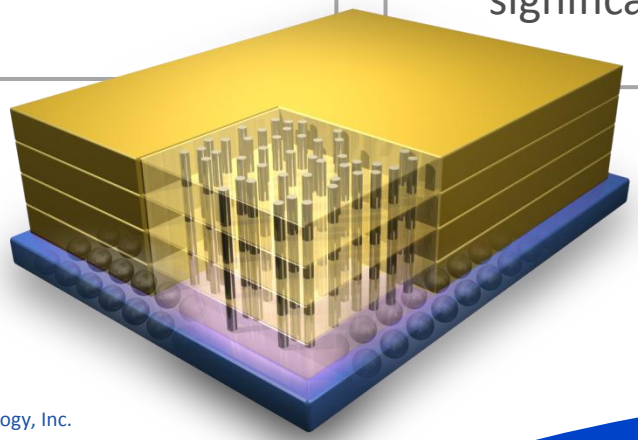
Through-Silicon Via (TSV) Assembly

Innovative Design & Process Flow

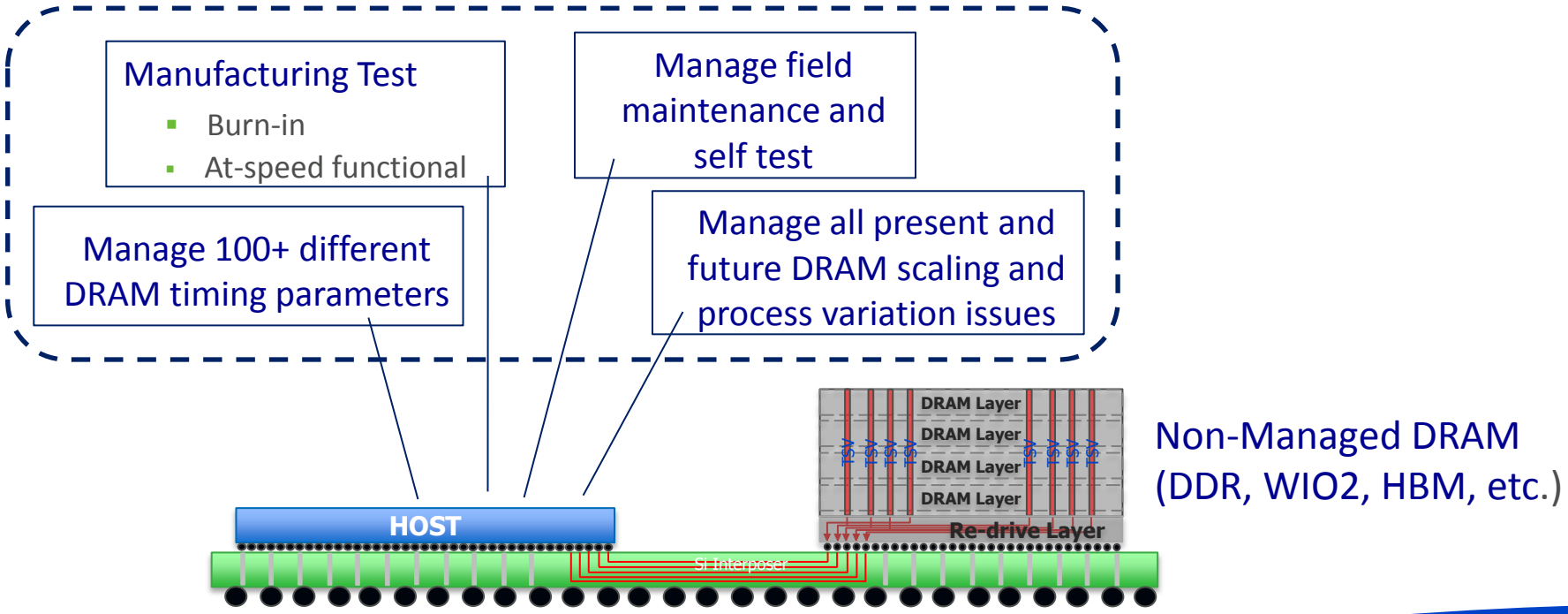
- Incorporates thousands of TSV sites per die to reduce signal lengths and power
- Enables memory scalability through parallelism

Sophisticated Package Assembly

- Provides higher component density and significantly improves signal integrity



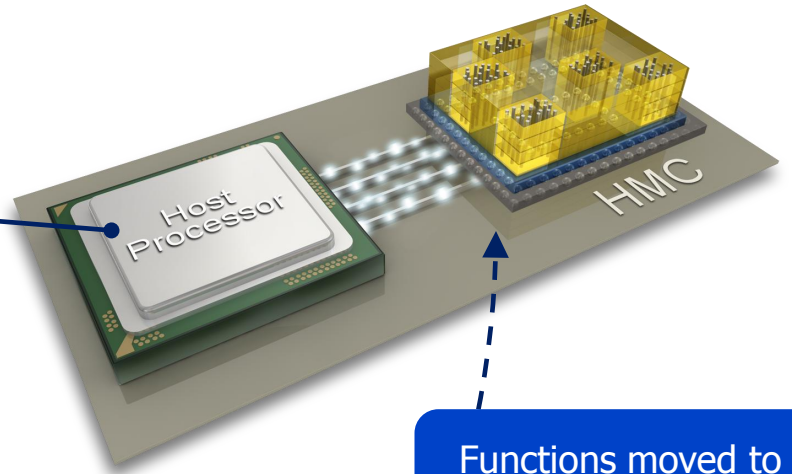
Traditional Host Processor Memory Management



Non-Managed DRAM (DDR, WIO2, HBM, etc.)

Simple HMC Memory Management

Simple memory requests
and responses;
No DRAM timings or scaling issues
to manage



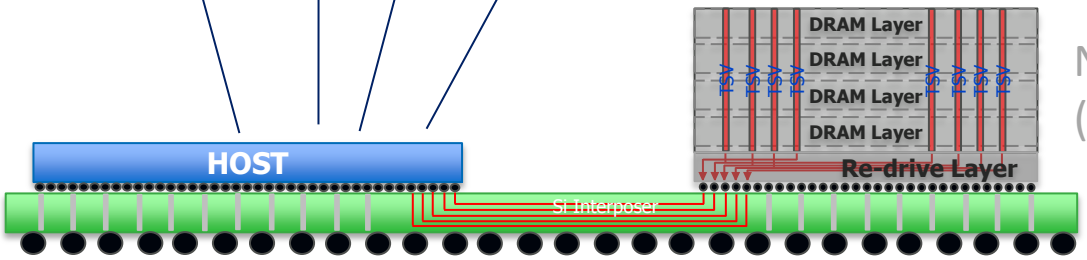
Functions moved to HMC for management

Manufacturing Test
- Burn-in
- At-speed functional

Manage field maintenance and self test

Manage 100+ different DRAM timing parameters

Manage all present and future DRAM scaling and process variation issues



Non-Managed DRAM
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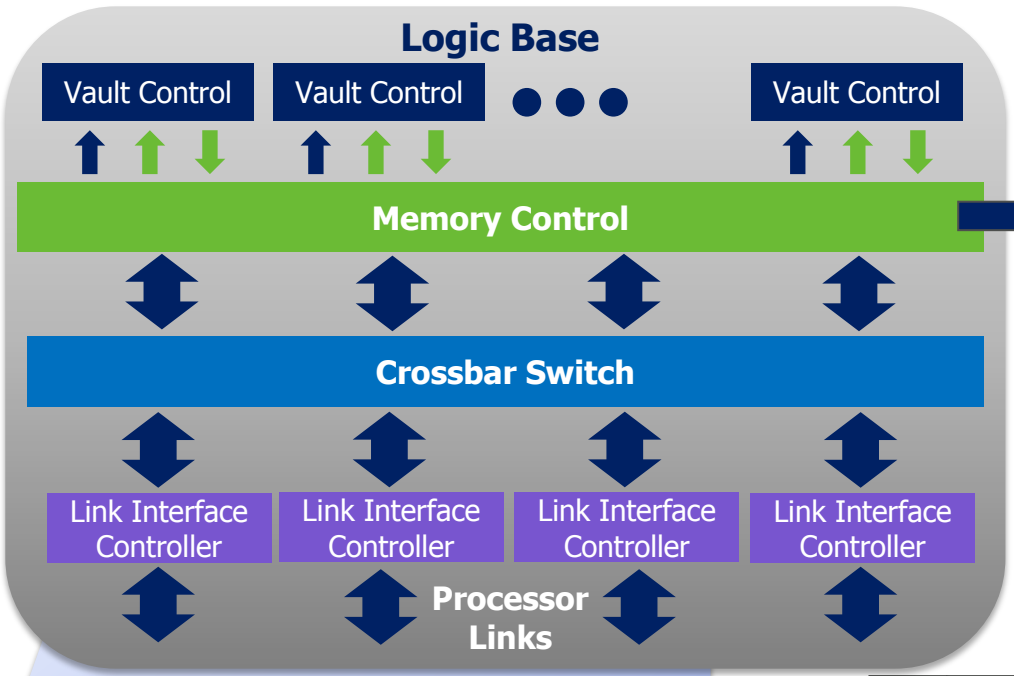
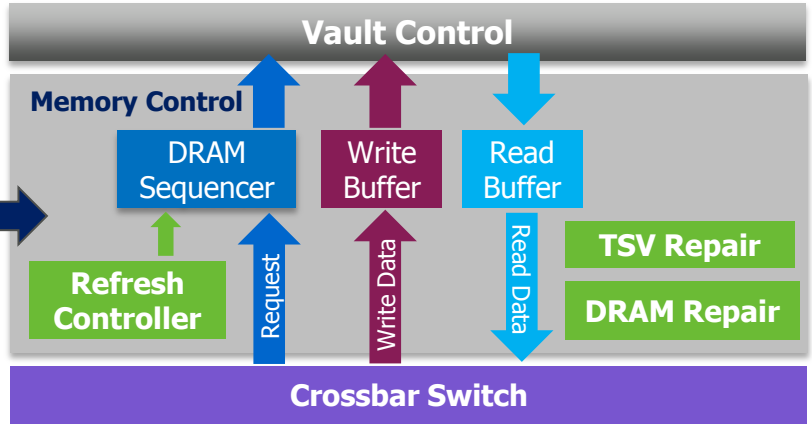
HMC Architecture

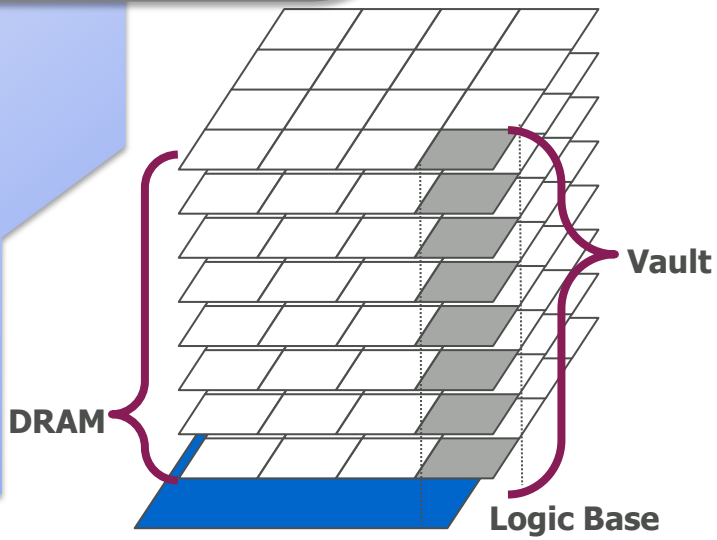




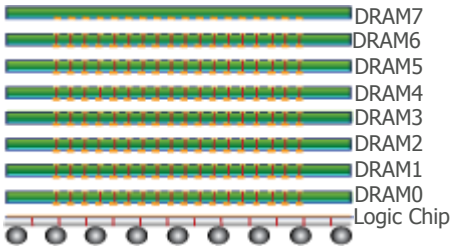
Detail of Memory Interface

Logic Base

- Multiple high-speed local buses for data movement
- Advanced memory controller functions
- DRAM control at the memory rather than at distant host controller
- Reduced memory controller complexity and increased efficiency



3DI & TSV Technology



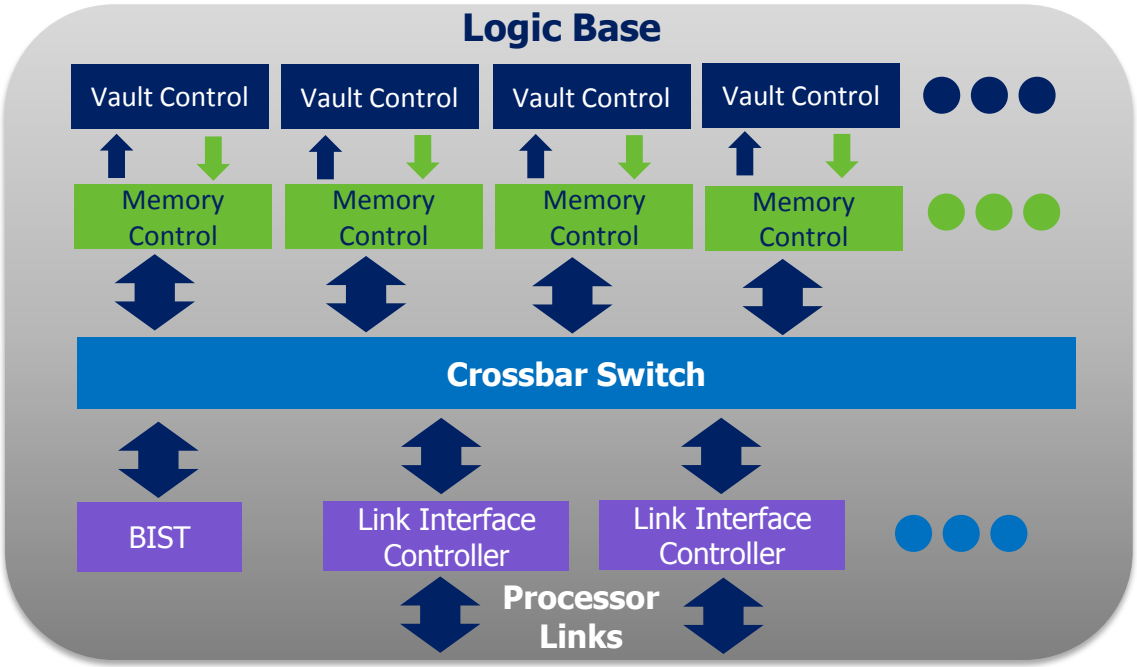
Vaults are managed to maximize overall device availability -

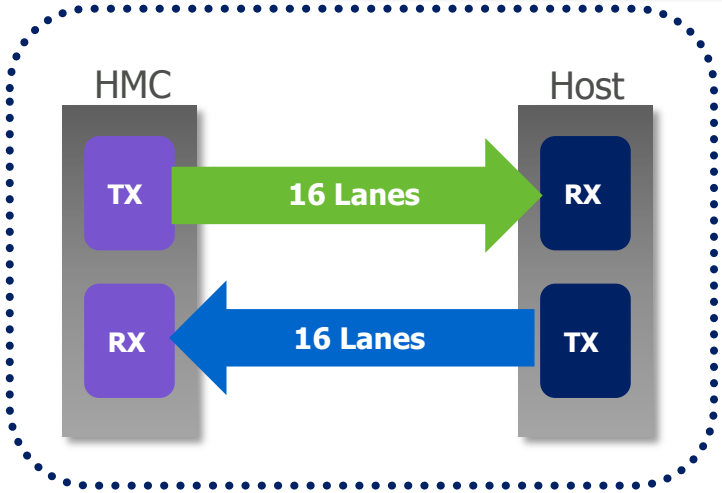
- Optimized management of energy and refresh
- Self test, error detection, correction, and repair in the logic base layer

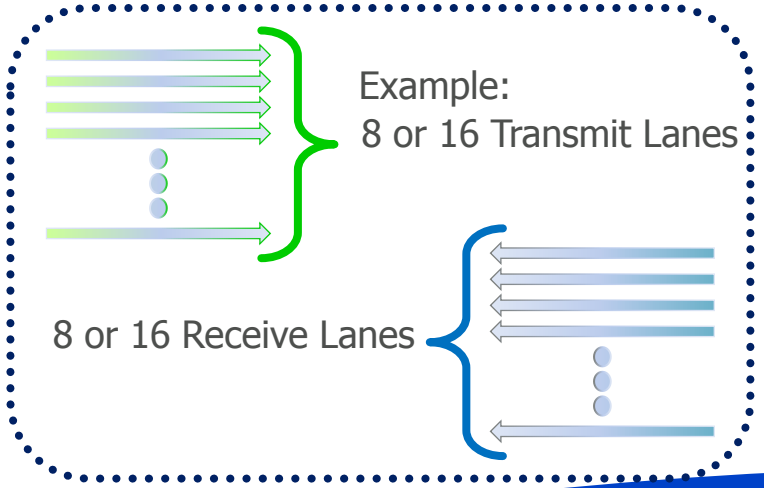
HMC Architecture

Link Controller Interface

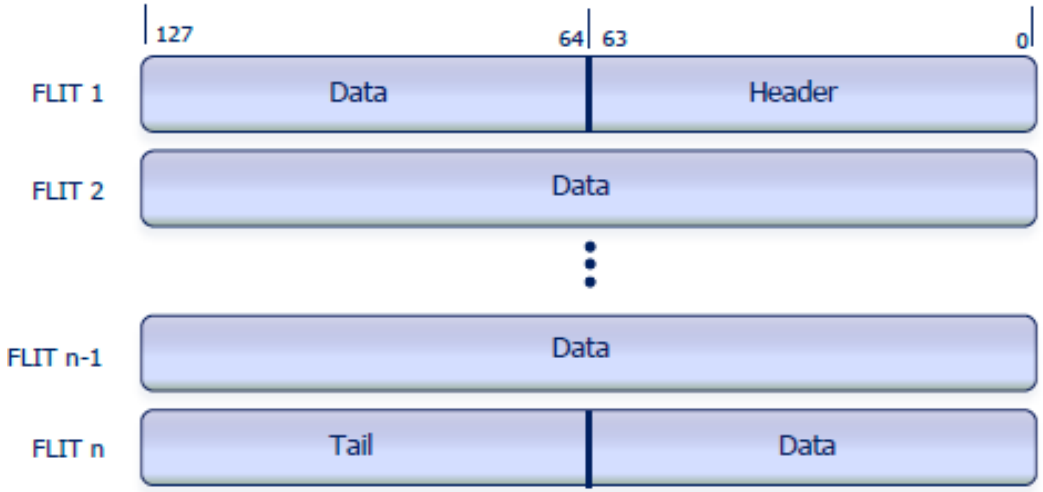
HMC-SR Options:
10 Gb/s, 12.5 Gb/s, or 15 Gb/s







Packet-Based Communication



Protocol NOT affected by any DRAM-related timings, nor is it DRAM-specific!

Packets comprised of 128-bit (16-byte) FLITs

- Packets include 1 to 9 FLITs, depending on command

Host issues requests & HMC issues responses

Each packet contains 64-bit header and 64-bit tail (1 FLIT)

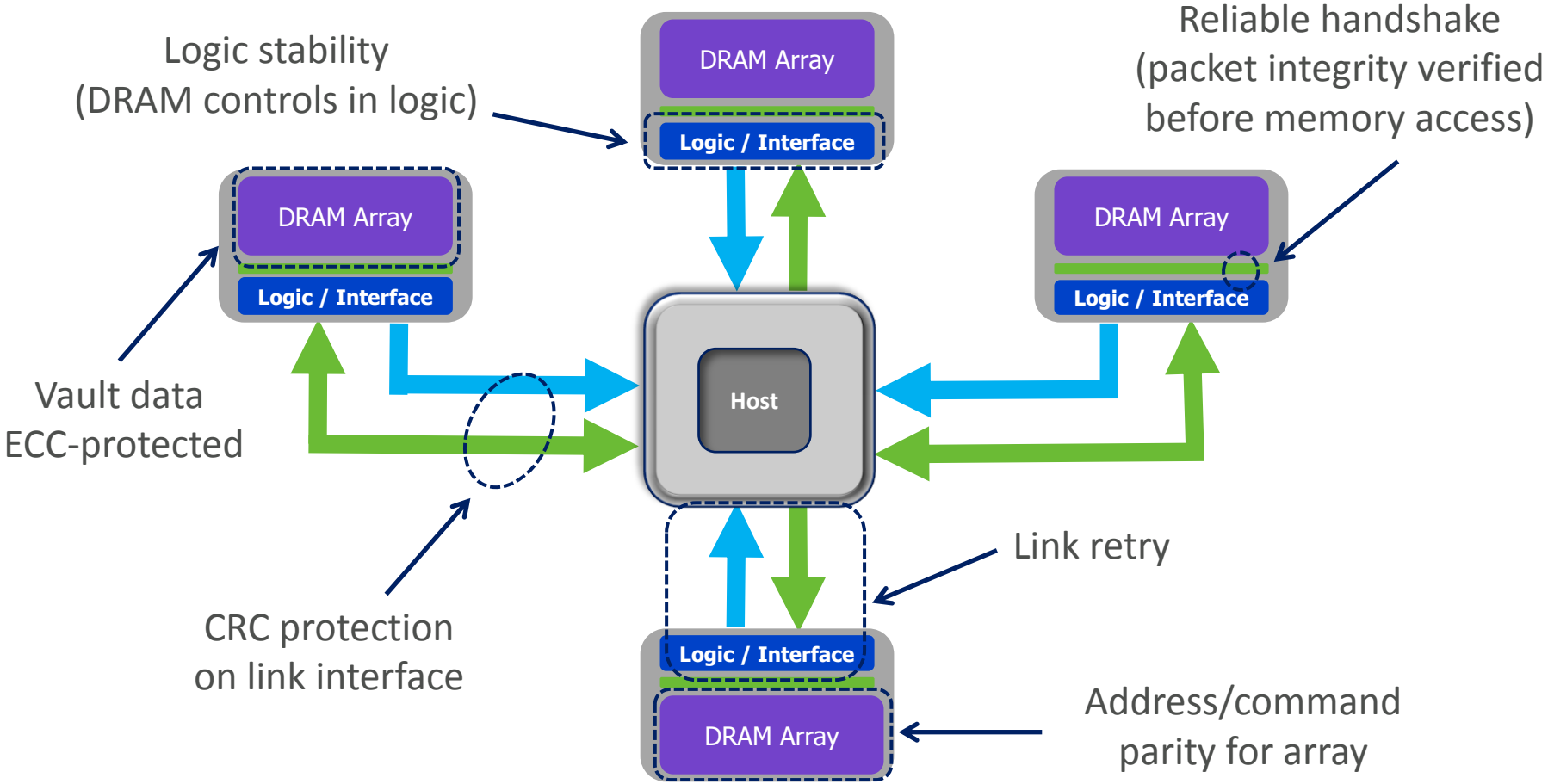
Multiple data transfer sizes supported (16B to 128B)

Commands include reads, writes, atomics, error responses

- Simultaneous READs and WRITEs supported

HMC Reliability

Built-in RAS features



RAS Feature System Comparison

FEATURE	DRAM	RDIMM	HMC
Extensive Test Flow	✓		✓
Data ECC		✓	✓
Address/Command Parity		✓	✓
Mirroring (back-up memory)			✓✓
Sparing (Chipkill)			✓✓
Lockstep (redundancy w/better ECC)			✓✓
CRC Coding			✓
Self Repair			✓
BIST			✓
Error Status and Debug Registers			✓
DIMM Isolation (flags faulty DIMM)			✓✓
Memory Scrubbing			✓

✓Supported ✓✓Redundant or not needed

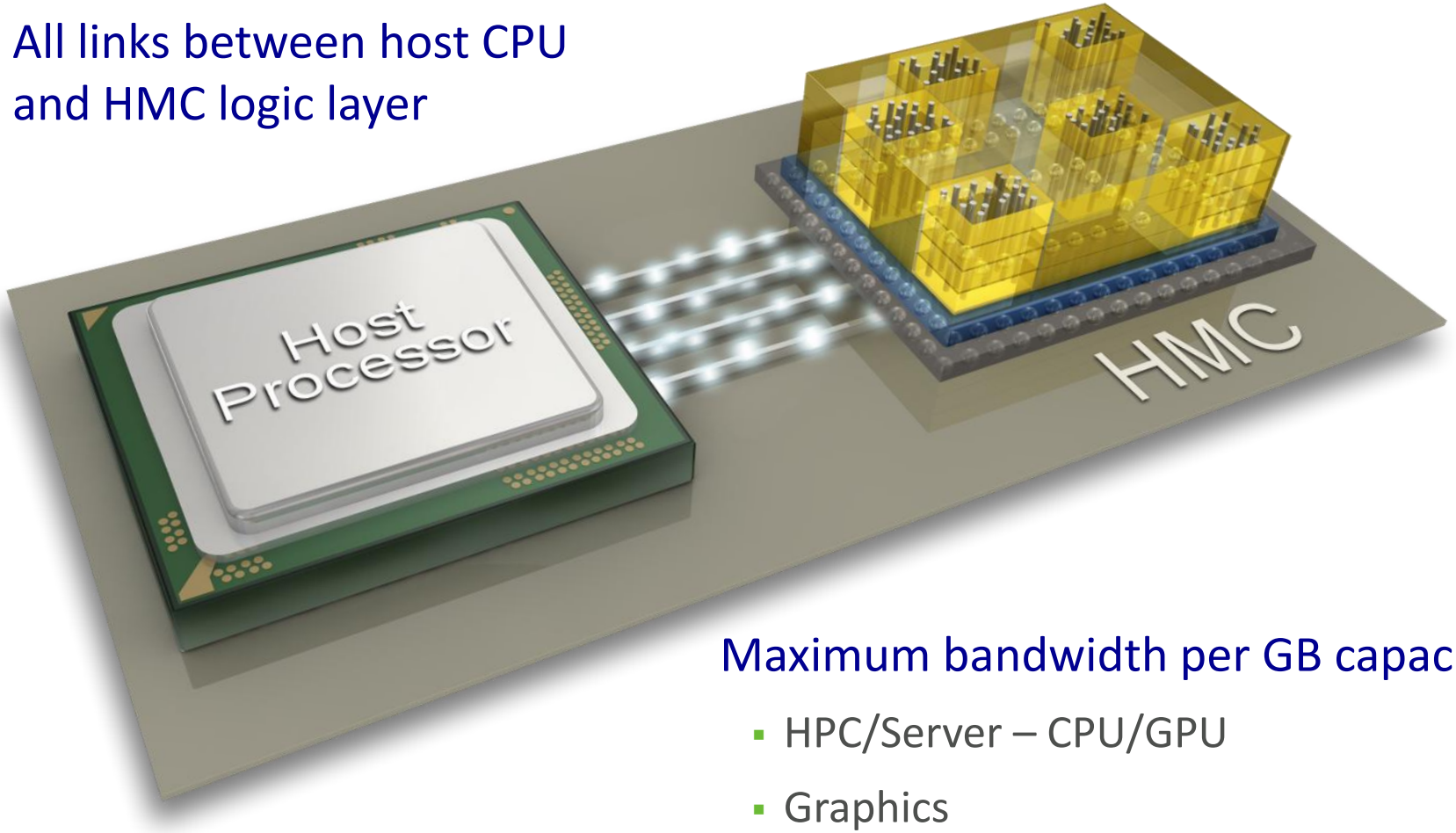
HMC Standard Packages

Up to 1.28 Tb/s memory
bandwidth available TODAY!

Standard BGA packaging solutions:
Cost-effective packaging using existing ecosystems
MCM and In-Package options available

HMC Maximum Bandwidth Configurations

All links between host CPU and HMC logic layer



Maximum bandwidth per GB capacity:

- HPC/Server – CPU/GPU
- Graphics
- Networking systems
- Test equipment

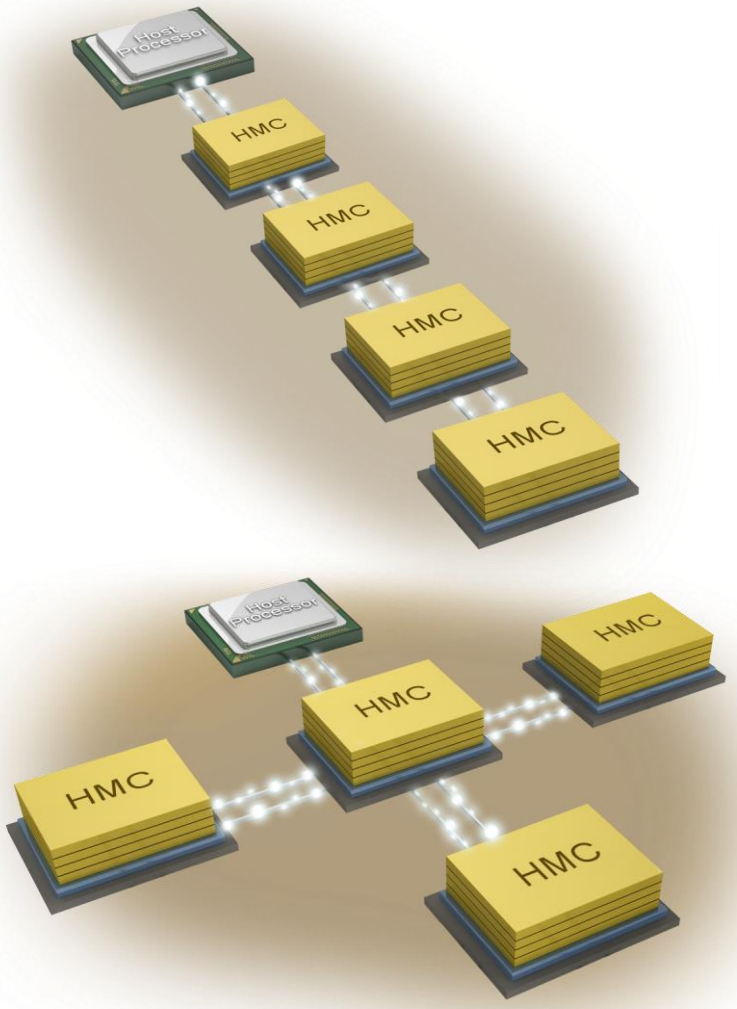
HMC Scalable Memory Solutions

Far Memory:

- Some HMC links connect to host – some to other cubes
- Scalable to meet system requirements
- Available in module form or soldered-down
- Building blocks for multiple application needs

Future Products May Include:

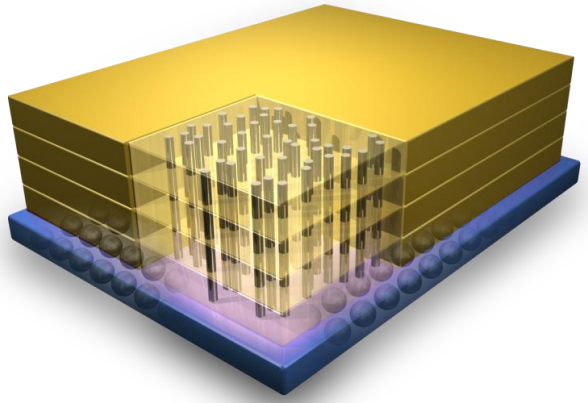
- Higher-speed electrical (SERDES) VSR-30
- Optical interfaces (align to industry stds.)
- Higher stack count for greater capacity
- Non-DRAM memory technologies
- Additional Atomic Operations inside Cube



Hybrid Memory Cube

Micron Memory Innovation

We've combined fast logic process technology and advanced DRAM designs to create an entirely new category of memory. Hybrid Memory Cube (HMC) technology provides a high-bandwidth, low-energy, high-density memory system that's unlike anything on the market today.



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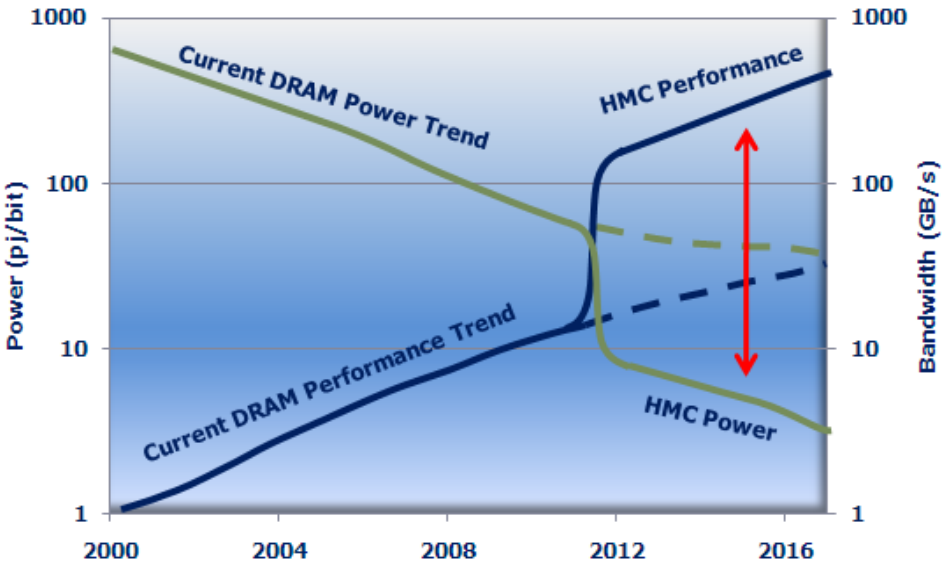

Unprecedented Performance

HMC will provide a revolutionary performance shift that will enrich next-generation networking and enable exaflop-scale supercomputing:

Reduced Power
Fraction of the energy per bit

Reduced Footprint
90% less space than today's RDIMMs

Increased Bandwidth
15X the performance of DDR3*

* HMC SR-15G vs. DDR3-1333

Industry Validation

"…unprecedented levels of memory performance"
- Electronic News

"…like adding a turbocharger to your computer"
- datacenteracceleration.com

"…get ready for some serious bandwidth to hit us in the near future"
- tweaktown.com

EE Times 40th Anniversary: "one of the top ten technologies expected to redefine the industry"

Consortium Momentum

ALTERA
ARM
IBM
Micron
Open-Silicon
SK hynix
SAMSUNG
XILINX

Hybrid Memory Cube CONSORTIUM

http://www.hybridmemorycube.org

Over 130 adopters to date and growing!

Milestones

2/11 - Micron announces the development of HMC technology

9/11 - Micron and Intel demonstrate Micron's HMC Gen1 device and an Intel MIC CPU memory interface at IDF 2011

12/11 - HMC wins Linley Group's Analyst Award for Best New Technology of 2011

4/13 – HMC named Memory Product of the Year

9/13 – Micron sampling 2GB HMC device

9/13 - Micron and Altera demo industry's first FPGA and HMC interoperability

11/13 – HMC part of Fujitsu next-gen supercomputer

4/14 - HMC Stratix V Team named Design Team of the year

2011 | 2012 | 2013 | 2014

10/11 - Micron and Samsung launch the HMC Consortium with fellow developers Altera, Open-Silicon, and Xilinx

12/11 - IBM joins the HMCC as a developer

5/12 - ARM and SK Hynix join the HMCC as developers

5/12 - HMC Spec 1.0 released to adopters for review

12/13 – HMCC Developer Group membership final – ARM, Altera, IBM, Micron, Open-Silicon, Samsung, SK Hynix and Xilinx

4/13 – HMCC releases final HMC Spec 1.0 to public

10/13 – HMCC adopter membership tops 120

2/14 - HMC Spec 2.0 released to adopters for review

HMC - A Revolutionary Shift

Increased Bandwidth

Greater Power Efficiency

Lower TCO

Reduced System Latency

Smaller, Scalable and Flexible

MICRON HMC

Thank You!


Micron®
Focused on Memory | Engineered for your Innovation