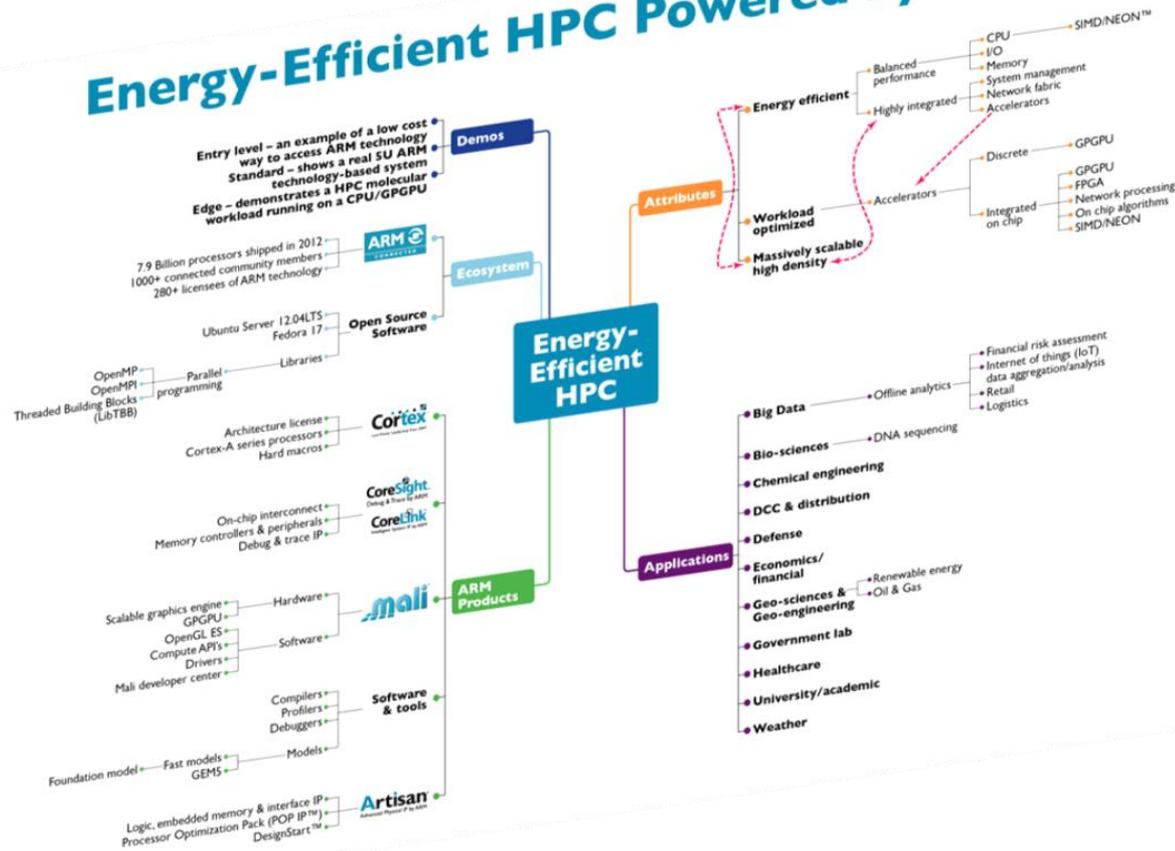


# Energy-Efficient HPC Powered by ARM®



**A balanced approach to BIG Data  
(using COTS-on-Silicon)**

- **What is today's agenda?**
  - introduction
  - economics
  - terminology
  - technology
  - direction

# introduction



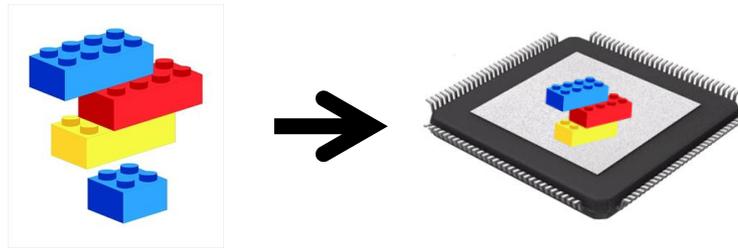
# INTRODUCTIONS

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- **Andrew N. Sloss** : [andrew.sloss@arm.com](mailto:andrew.sloss@arm.com)
  - Seattle, Senior Principal Engineer
  - Marketing, Strategic Alliances
- **Nigel C. Paver** : [nigel.paver@arm.com](mailto:nigel.paver@arm.com)
  - Austin, ARM Fellow
  - R&D, Leading R&D HPC activity in ARM
- **Eric Van Hensbergen** : [eric.vanhensbergen@arm.com](mailto:eric.vanhensbergen@arm.com)
  - Austin, Principal Design Engineer
  - R&D, ARM Research for US/HPC

## ■ SHIFT

- No longer solely rely on **Process Reduction** to improve performance
- Performance/Power/Cost will increasingly become reliant on **Integration**



## ■ ARM

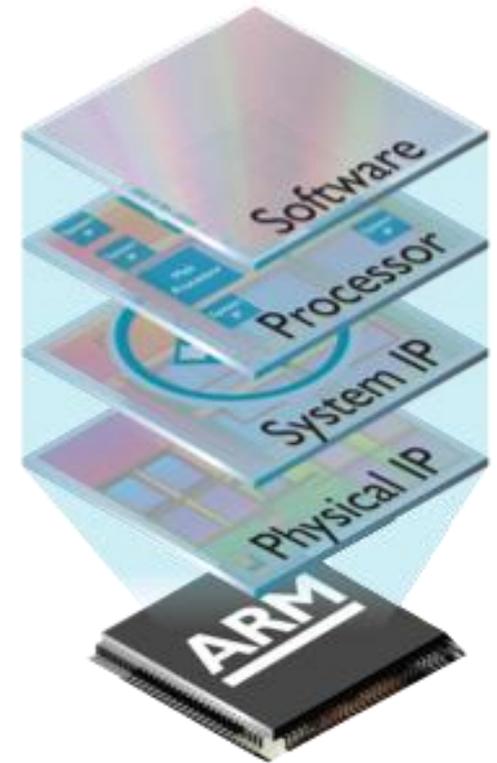
- Focuses on Design & Licensing of IP Building Blocks for SoCs (=LEGO's)
- Fosters an eco-system of standard pieces, acting as *COTS-on-Silicon*
- *COTS-on-Silicon* encourages multi-suppliers through the eco-system
- Allowing the eco-system the ability to deliver cost effective solutions
  - Enforcing localized optimized end designs
- Enabling circuit-boards to be miniaturized onto a single chip
- While retaining the technology DNA of Energy-Efficiency

# economics



## ■ Build what you want?

- Target your SoC to solve your problem
  - One size does not fit all
  - Optimize power/performance for the domain
- Utilize common infrastructure and components
  - Leverage SW ecosystem and portability
  - Leverage validated IP
  - Proven design flows
- Focus on adding value to solve your problems
  - Adding you application specific IP
  - Everything else off the shelf
    - Rich IP libraries
- Diverse and competitive IP vendors
  - Leverage the ARM ecosystem



## ■ What are the ARM numbers?

- ARM “the company” : **>22-years**
- Processors shipped in 2012 : **~8.7 Bu (~7.9 Bu`11)**
- Processors shipped in total : **>38 Bu**
- Processor licenses : **~960**
- Semiconductor partners : **310**
- Foundry partners : **5+**
- Process technology : **14 – 250 nm**
- Connected community members : **1000+**

# COLLABORATION

## Silicon Partners



## Design Support Partners



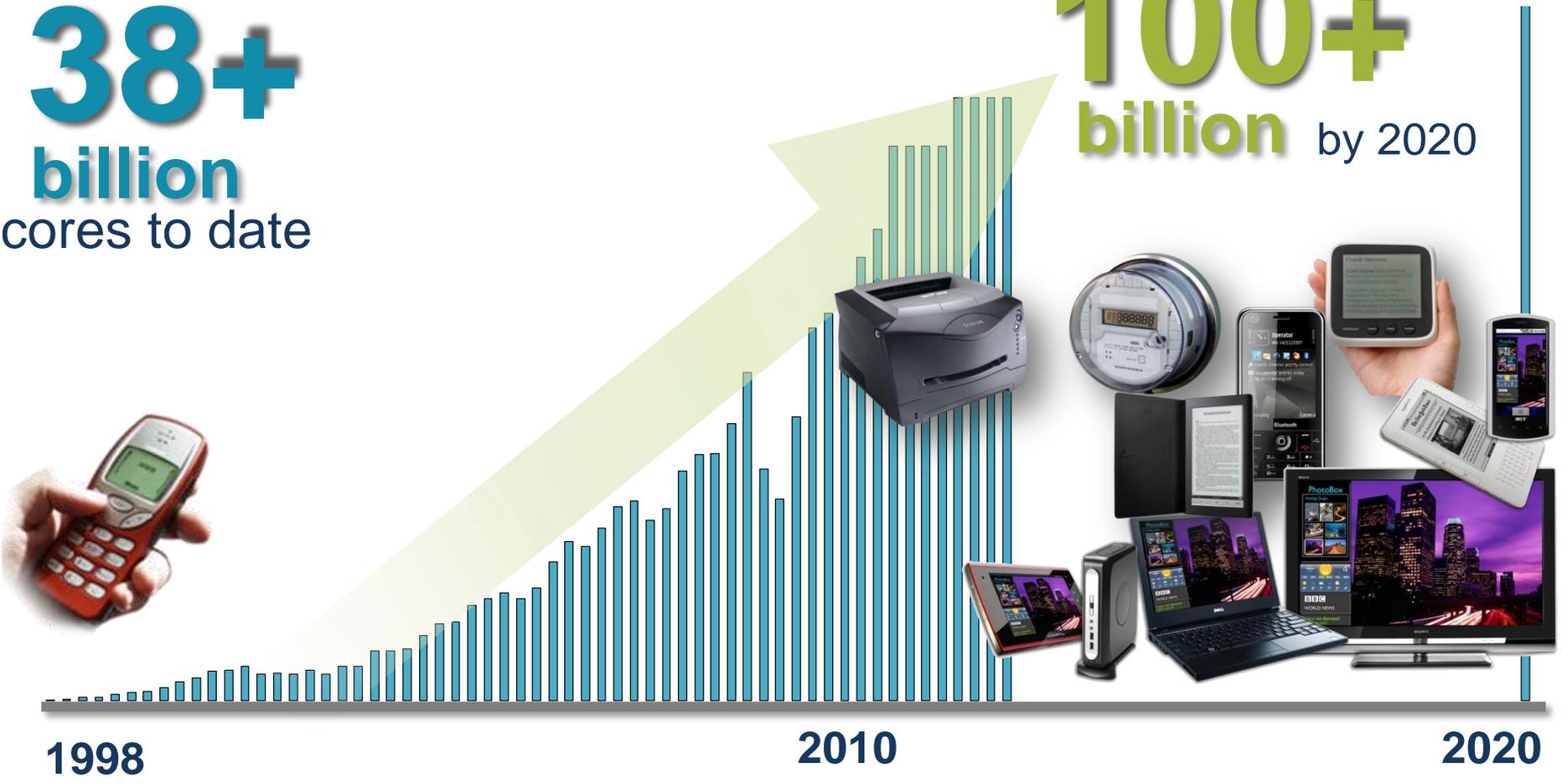
## Software, Training and Consortia Partners



# COTS-on-Silicon

**38+**  
billion  
cores to date

**100+**  
billion by 2020



# MARKETS

**Mobile** **4.6bn** in 2011



**Home** **0.4bn** in 2011



**Embedded** **2.3bn** in 2011



**Enterprise** **1.4bn** in 2011



# terminology



# PROCESSORS

## Architecture "ARMv8"

ARM<sup>®</sup> Architecture  
Reference Manual  
ARMv7-A and ARMv7-R edition

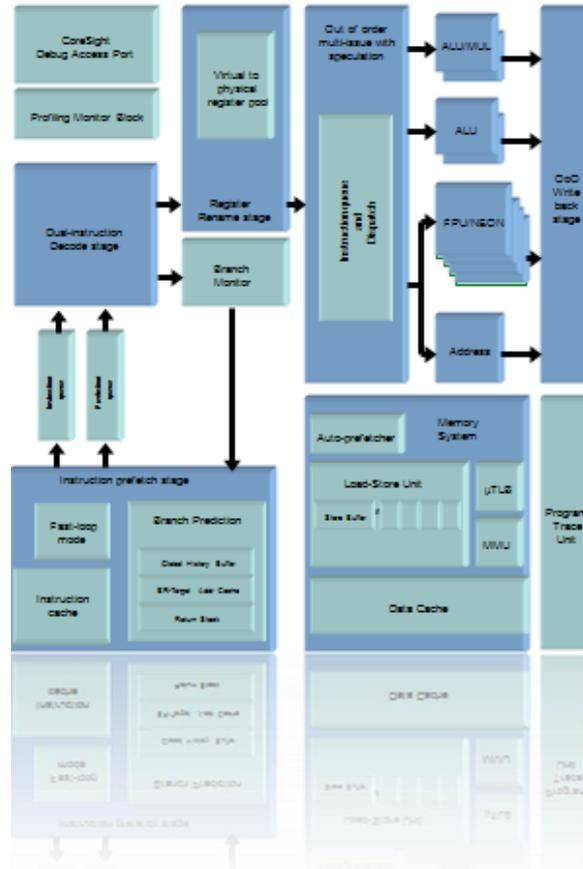
**ARM<sup>®</sup>**

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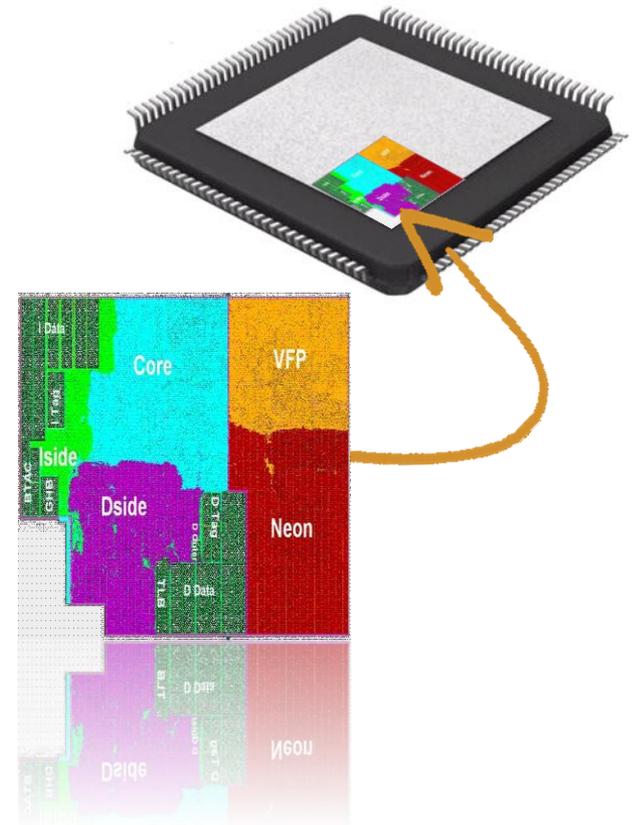
ARM DDI 0406B\_errata\_2010\_Q3 (ID100710)  
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**ARM<sup>®</sup>**

## Processor Micro-Architecture "Cortex-A57"



## Processor Hard-Macro Implementation



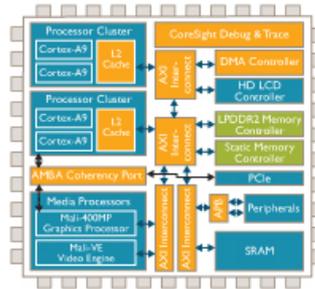
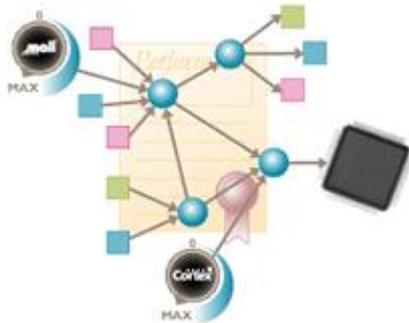
# technology



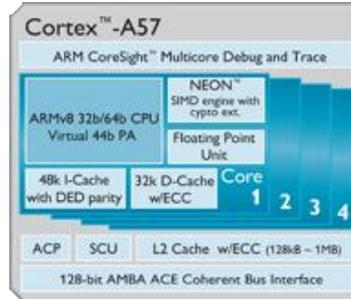
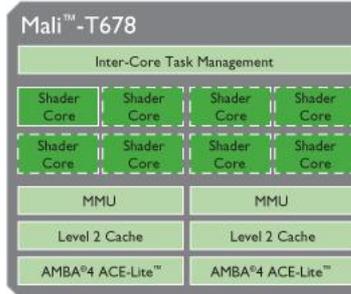
## Physical IP



## System IP



## Processor & Graphics IP



## Development Systems (software)



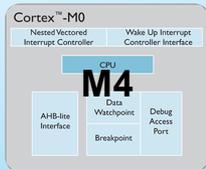
# SPECTRUM

## Cortex-M series (Microcontroller)

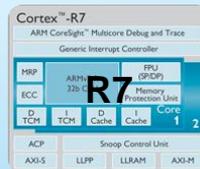
## Cortex-R series (Real Time)

## Cortex-A series (Application)

PERFORMANCE



28HPM  
800+ MHz  
+FP +DSP

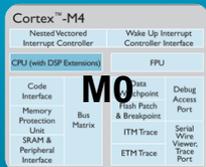


x2

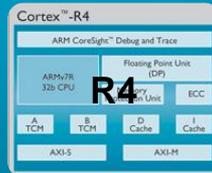
1+ GHz  
MP



2+ GHz  
64-bit  
Fully OoO



40G  
4 uW/Mhz  
0.01 mm<sup>2</sup>  
12K Gates



40LP  
0.071mW/MHz  
0.18 mm<sup>2</sup>

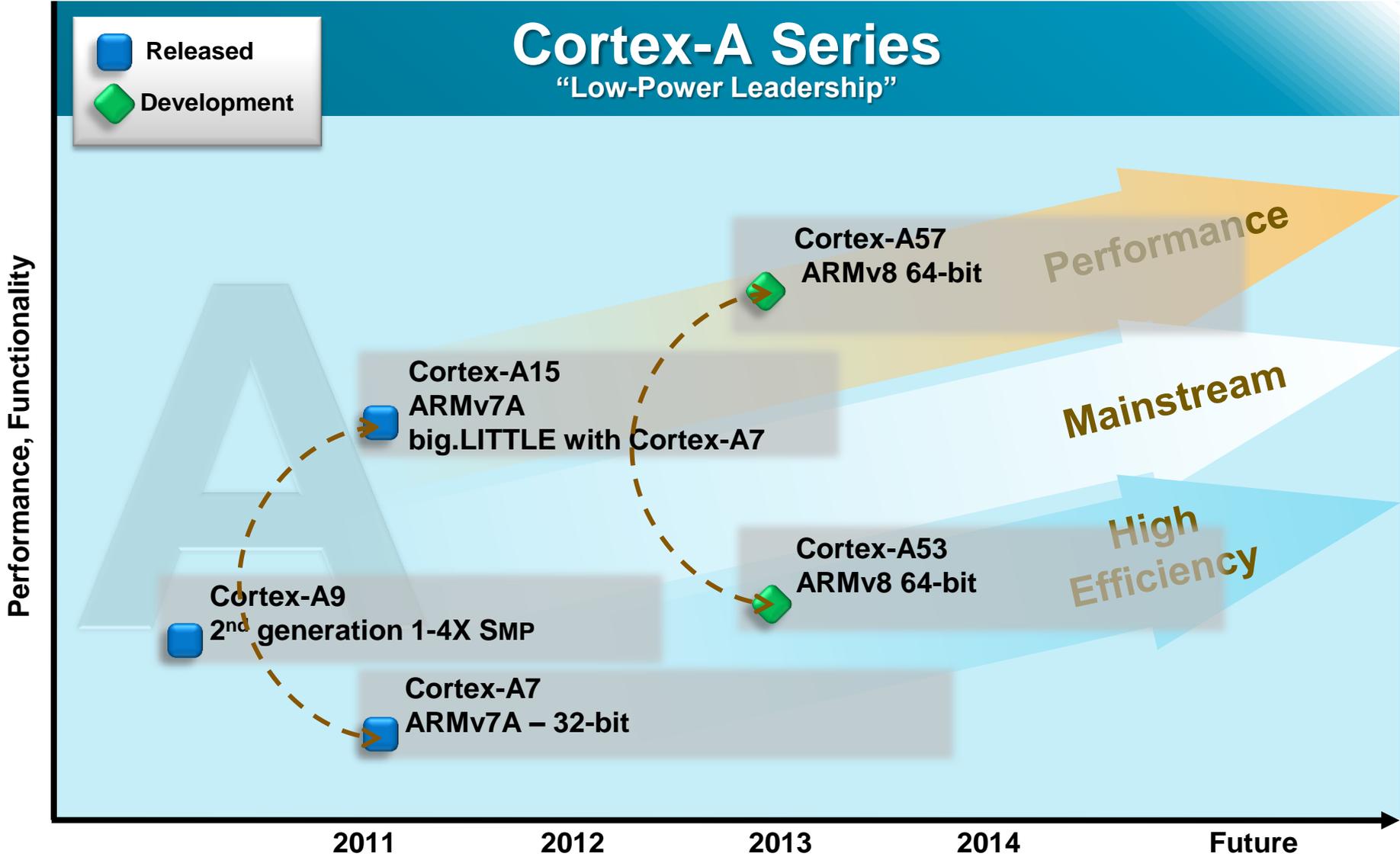


40LP  
0.12mW/MHz  
0.68 mm<sup>2</sup>

POWER EFFICIENCY

**Note:** the numbers may vary depending on specific implementation details

# ROADMAP



# direction



- **ARM is aiming for a balanced approach?**
  - Bring the advantages balanced technology into new areas
  - Technology has to balance performance, power and area (=cost)
  - Efficiency through a careful technology balance e.g. big.LITTLE solutions
  - Companies can select the right PPA\* fit-for-purpose
  - Stacked die : CPU+MEMORY+IO
  - Adopting new memory technologies/interfaces:
    - emerging non-volatile technology
  - Balancing the new and old workloads
    - Old: SIMD / Fortran / Vectorizing
    - New: Map-reduce and beyond / Sparse Matrices / Pointer Chasing

PPA : Power Performance Area

# summary



## ■ What to take away?

- No longer solely rely on Process Reduction to improve performance
- Performance/Power/Cost will increasingly become reliant on Integration
- ARM designs and licenses IP building blocks for >22-years
- IP Business Model fosters a eco-system of tested components
- Allowing tailored solutions to be created for HPC/Big Data problems
- Building Blocks include Processor IP, Physical IP, System IP & Software
- Bringing the cross-pollination balanced technology from other segments
- *COTS-on-Silicon* encourages multi-suppliers throughout the eco-system
- Eco-system can deliver cost effective solutions in sensitive markets
  - Enforcing localized optimized end designs

## Energy Efficiency Underlies It All





**end**

