AMD
Smarter Choice

V & V @ AMD: Ensuring a Solid HPC Foundation and Data Confidence from Core to Cache and Beyond . . .

Seth Prejean
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```
*** STOP: 0x0000001E (0xC0000005,0x80101E08,0x00000000,0x0B000001)
KMODE_EXCEPTION_NOT_HANDLED*** Address 80101e08 has base at 80100000 - ntoskrnl.
exe

p7-0108 irql:1f     SYSVER 0xf00002f4

Dll Base DateStmp - Name                 Dll Base DateStmp - Name
80100000 2e3d2e69 - ntoskrnl.exe         80400000 2e35a15f - hal.dll
801e2000 2e39c53d - setupdd.sys          80014000 2e2f2258 - SCSIPORT.SYS
8001c000 2e36bab2 - vga.sys              80212000 2e394943 - VIDEOPRT.SYS
80216000 2e2f2240 - floppy.sys           80216000 2e2f2242 - i8042prt.sys
80222000 2e2f2245 - kbdclass.sys         80225000 2e3c24a1 - fastfat.sys
fcc00000 2e2f21fc - fd16_700.sys

Address  dword dump   Build [756]                              - Name
fde1466c 80101e08 80101e08 00000000 0b000001 80134876 fde1469c - ntoskrnl.exe
fde14678 80134876 80134876 fde1469c 80136e73 fde146a4 00000000 - ntoskrnl.exe
fde14680 80136e73 80136e73 fde146a4 00000000 fde146a4 fde1492c - ntoskrnl.exe
fde146a8 8013eaca 8013eaca fde1492c fde14f6c fde14768 fde14748 - ntoskrnl.exe
fde146c0 8013eade 8013eade fde14f6c fde1474c 80124b34 fde1492c - ntoskrnl.exe
fde146cc 80124b34 80124b34 fde1492c fde14f6c fde14768 fde14748 - ntoskrnl.exe
fde146e0 80136e2c 80136e2c 0b000001 0b000001 fde14940 0b000001 - ntoskrnl.exe
fde146fc 80101e12 80101e12 00000008 00010286 fde148d0 00000010 - ntoskrnl.exe
fde14714 80136e2c 80136e2c e1000828 80187c96 e1000828 00000468 - ntoskrnl.exe
fde1471c 80187c96 80187c96 e1000828 00000468 fde14780 00000246 - ntoskrnl.exe
fde14730 80102053 80102053 fde148a8 8011d7a8 fde14980 fde13000 - ntoskrnl.exe
fde14738 8011d7a8 8011d7a8 fde14980 fde13000 fde14f90 00000000 - ntoskrnl.exe
fde14750 8011f1a7 8011f1a7 fde1492c fde14768 0b000001 0b000001 - ntoskrnl.exe
fde1478c 801105c9 801105c9 e102300c c038408c fe3ea120 00000000 - ntoskrnl.exe
fde147b4 801050fd 801050fd e102300c c038408c 00000000 fdeaab70 - ntoskrnl.exe
fde147e0 80136e2c 80136e2c 80198c58 ffffffff fde1485c 8013acb1 - ntoskrnl.exe
fde147e4 80198c58 80198c58 ffffffff fde1485c 8013acb1 00000000 - ntoskrnl.exe
fde147f0 8013acb1 8013acb1 00000000 00000030 00000023 00000023 - ntoskrnl.exe
fde14820 80101e08 80101e08 00000008 00010203 fde149f4 00000010 - ntoskrnl.exe
fde1484c 8013d077 8013d077 00000001 0b000005 8013d1e5 fded0ba8 - ntoskrnl.exe
fde14858 8013d1e5 8013d1e5 fded0ba8 00000023 00000001 00000023 - ntoskrnl.exe
fde14878 8010fd6c 8010fd6c fded0788 00000023 00000001 00000000 - ntoskrnl.exe
fde148c4 80101e12 80101e12 00000008 00010286 e1022740 fde14944 - ntoskrnl.exe
fde14904 80136e2c 80136e2c 80198c58 ffffffff fde14980 8013acb1 - ntoskrnl.exe
fde14908 80198c58 80198c58 ffffffff fde14980 8013acb1 fde1492c - ntoskrnl.exe
fde14914 8013acb1 8013acb1 fde1492c 00000000 fde14980 00000000 - ntoskrnl.exe
fde14938 80101e08 80101e08 00000002 00000000 0b000001 0b000001 - ntoskrnl.exe
fde1495c 80137604 80137604 c0000005 00000001 fd014bd8 fde14980 - ntoskrnl.exe
fde14970 8013d077 8013d077 00000000 0b000001 8013d1e5 00000246 - ntoskrnl.exe

Restart and set the recovery options in the system control panel
or the /CRASHDEBUG system start option. If this message reappears,
contact your system administrator or technical support group.
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V & V @ AMD

Verification (Pre-Silicon)

- Ensure logical functionality of the design
- Simulation environment
  - RTL
  - Process Modeling
  - Thermal CFD Modeling

Validation (Post-Silicon)

- Ensure the product meets design specifications
- System environment
  - Automated Test Equipment
  - System Level Test
  - Burn In

Confidence In Simulations

How do we provide confidence in predictive simulations ?

- We must ensure data is reliable within our design
- V & V can ensure data will be processed correctly
- Data must be protected from corruption
- Prevent conditions for data corruption
- Unavoidable corruption is detected and in some cases corrected

Reliable Data

What affects data reliability in a complex microprocessor?

- Soft Errors
  - Cosmic upsets
  - Alpha particle strikes
- Temperature
  - Timing margin
  - Test temperature coverage
- Power supply Noise
  - Glitches on power supplies
  - Power Grid Design

Reliable Data

Soft Errors

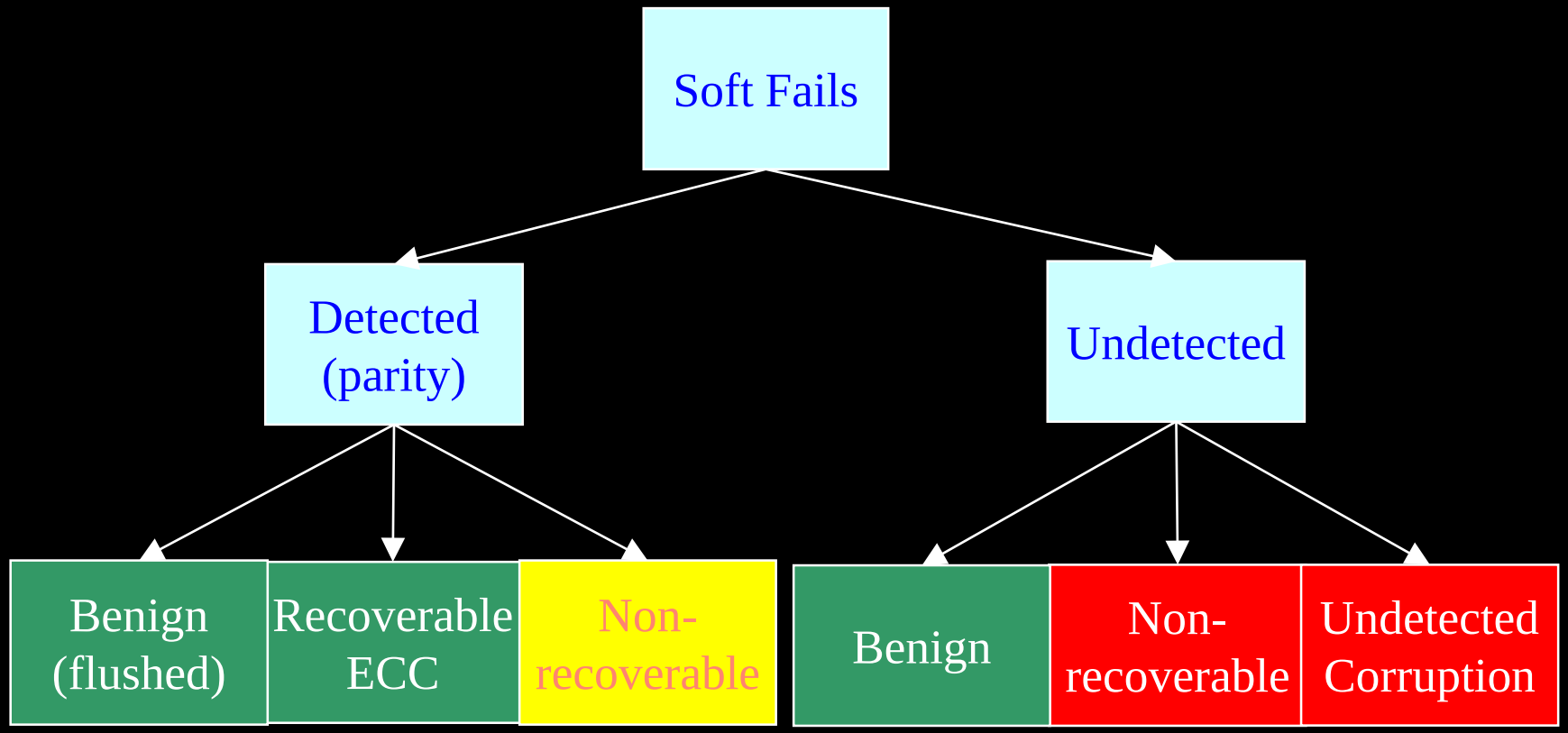
- Scaling reduces Qcrit while also reducing collection volume
- Increase in number of storage nodes on a device
- Multiple cores impact total device FIT

Mitigation

- Protect data with ECC and parity
- Report and repair errors with Machine Check Architecture
- Control and monitor process materials to ensure they are alpha emission free

Reliable Data

Classifying Soft Fails



Reliable Data

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Soft Errors

- Taxonomy of Systems Effects from Soft Errors

Perturbation (*2)	**Detection**	**Containment**	**Recovery**	**System Effects**
Unperturbed	-	-	-	***None***
Perturbed	Detected	Contained	Recovered	***Recovered***
			Unrecovered	***Local Failure*** (*3)
		Uncontained	-	***Global Failure***
	Undetected	-	-	***Silent Data Corruption***

Notes:
1. Each column can apply to any layer (HW, system SW, app SW, etc.).
2. Perturbation: Fault or upset becomes an error (i.e., does not vanish).
3. Local Failure: Scope and degree of failure depends on specific errors, mechanisms, and policies.

source: Dean Liberty; AMD RAS architect

Reliable Data

On Die Thermals

- Scaling increases power density
- Hotspot detection is important
- Device Thermal gradients in the silicon can affect timing and data reliability
- Thermal runaway
  - SIDD(Temp(SIDD)) – feedback between static leakage and temperature can induce self heating

Product Specifications ensure that these problems can be mitigated

Reliable Data

On Die Thermals

- Test Temperatures ensure thermal coverage
  - Understanding thermal profiles across device operation is critical
- Detection
  - Diodes measure device temperature
  - Distributed sensor networks can detect hot spots
- Prevention
  - HTC Hardware Thermal Control
    - Reduce frequency / voltage
  - Thermal Trip reset mechanism

Data Protection

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Hammer Family Data Protection

Prior history establishes protection structure and requirements; New design work extends coverage

- ECC and Parity
  - L1 Data Cache ECC protected
  - L2 Cache and Cache Tags ECC protected
  - DRAM ECC Protected (with Chipkil ECC support)
  - L1 Instruction Cache TLBs and Tags Parity Protected
  - Read only data that system can recover Parity Protected

Data Protection

Hammer Family Data Protection continues …

- Cache Scrubbers
  - Run in background checking and repairing data
  - Address range and scrub rate are configurable
- Machine Check Architecture
  - Reports failures and failure results
  - Enables hardware and software error containment
- Physical bit Layout Interleaving
  - ECC is SECDED
  - Interleaving eliminated possibility of double or N-bit errors within same logical word

Design Verification

RTL Design Verification of Data Protection

- Soft error injection scripts
  - ECC detection and correction
- Machine Check Architecture verification
  - Error reporting mechanism works
  - Valid data is reported to fail data registers

Design Verification

Thermal Design Verification

- Design CaC simulation for thermal density maps
- Thermal modeling to predict silicon device temperatures and gradients
- Max Power Test Pattern
  - Worst case power dissipation in a real world functional state
- Useful for
  - Sensor placement
  - Timing margin reliability in hot spots
  - Thermally aware design

Product Validation

Product DFT features enable validation of implemented reliability features

- Machine Check Architecture / Parity / ECC
  - Validate error reporting registers
  - MCA functionality
  - Inject bit flips during device operation

Product Validation

- Cosmic Soft Error Rates
  - Accelerated Soft Error Rate measurement
  - Los Alamos Neutron beam facility
  - Memory and Logic Flop/Latch FIT rates measured
  - System Level OS FIT rate measurement
    - Architectural Relevancy Factor
  - SER FIT rates are calculated at the product level

Product Validation

- Die Level Thermal Imaging
  - System level device thermal mapping across different applications
  - Thermal sensor validation/correlation
  - On Die thermal gradient measurement

Looking Forward

- Multi-core products increase the challenge of ensuring reliable data while offering improved performance and data throughput with same quality.
- Logic to dominate Soft Error FIT rates
  - SRAM FIT rates leveling off and well understood
  - SRAM data reliability mitigation is common practice
  - Logic data reliability is a new focus of development and will require checkpoint and logic ECC/parity mechanisms
- Design tradeoffs
  - Data protection such as ECC and parity or other logic protection schemes impact performance and increase chip area

Summary

- Challenges to ensure Data Reliability increase as semiconductor technology advances.
- Simulation and modeling are key to addressing issues and ensuring confidence in our processors.
- Validation confirms the effectiveness of measures taken to ensure product reliability.
- Legacy techniques and customer requirements/expectations drive implementation of reliability features.

Thanks to contributions taken from the work of:

Dean Liberty and Fred Weber

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