Reliability as a challenge & opportunity to technology scaling

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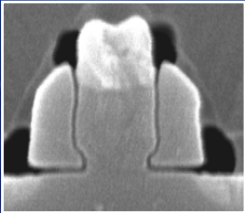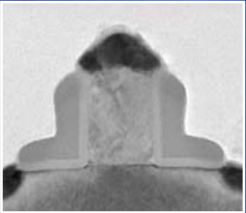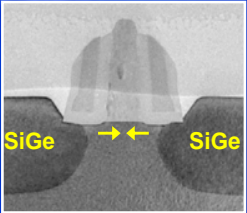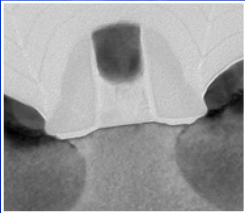**Director of Logic Technology Quality & Reliability**
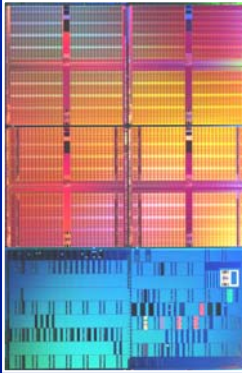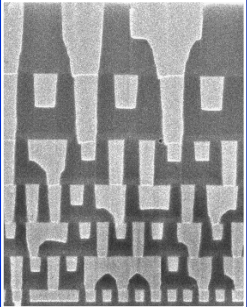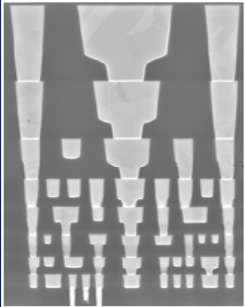
2007 Salishan HPC Conference
April 26, 2007

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Key Messages

- **Technology scaling continues according to Moore's Law**
  - 2X increase in functionality every 2 years
  - In the form of cores, integrated functionality or both
  - 65nm in 2005, 45nm 2007, 32nm 2009

- **Technology & Reliability Challenges are many, but so are the opportunities**
  - Many new device types and materials
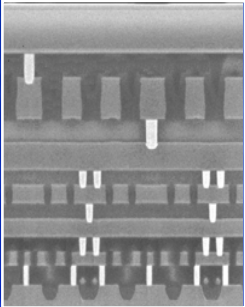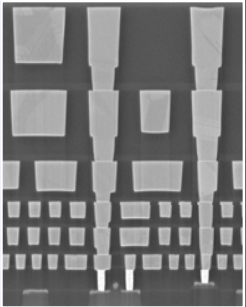 - A challenge as well as an opportunity

- **High RAS will require global fault management strategies along with robust circuit design**
  - Better understanding needed on RAS requirements
  - Research and Cost effectiveness of proposed options

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Technology scaling on a 2 Year Cycle

	180 nm	130 nm	90 nm	65 nm	45 nm
	1999	**2001**	**2003**	**2005**	**2007**

Transistor

Interconnect

200mm	300mm	300mm	300mm	Details
100nm L_G	70nm L_G	50nm L_G	35nm L_G	Coming!
$CoSi_2$	$CoSi_2$	NiSi	NiSi	
		Strain Si	2nd Strain	
6 Al	6 Cu	7 Cu	8 Cu	
SiOF	SiOF	Low-k	Low-k	**Courtesy: Intel**

SiGe → ← SiGe

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Moore's Law Delivers Value to the End User
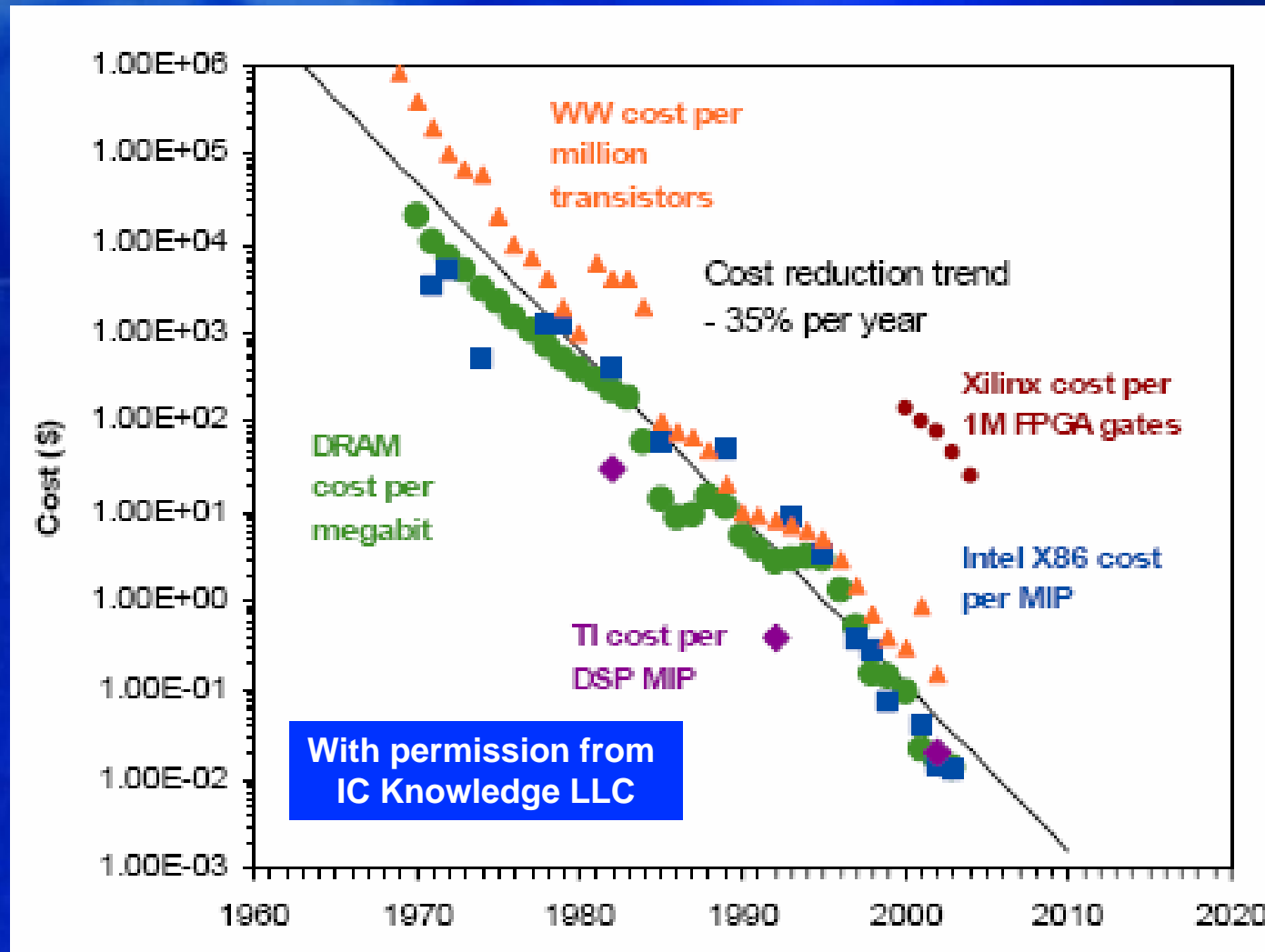
Twice the functionality at the same cost every 2 years

Performance/ Watt

Trend in Performance/ Watt relative to i386
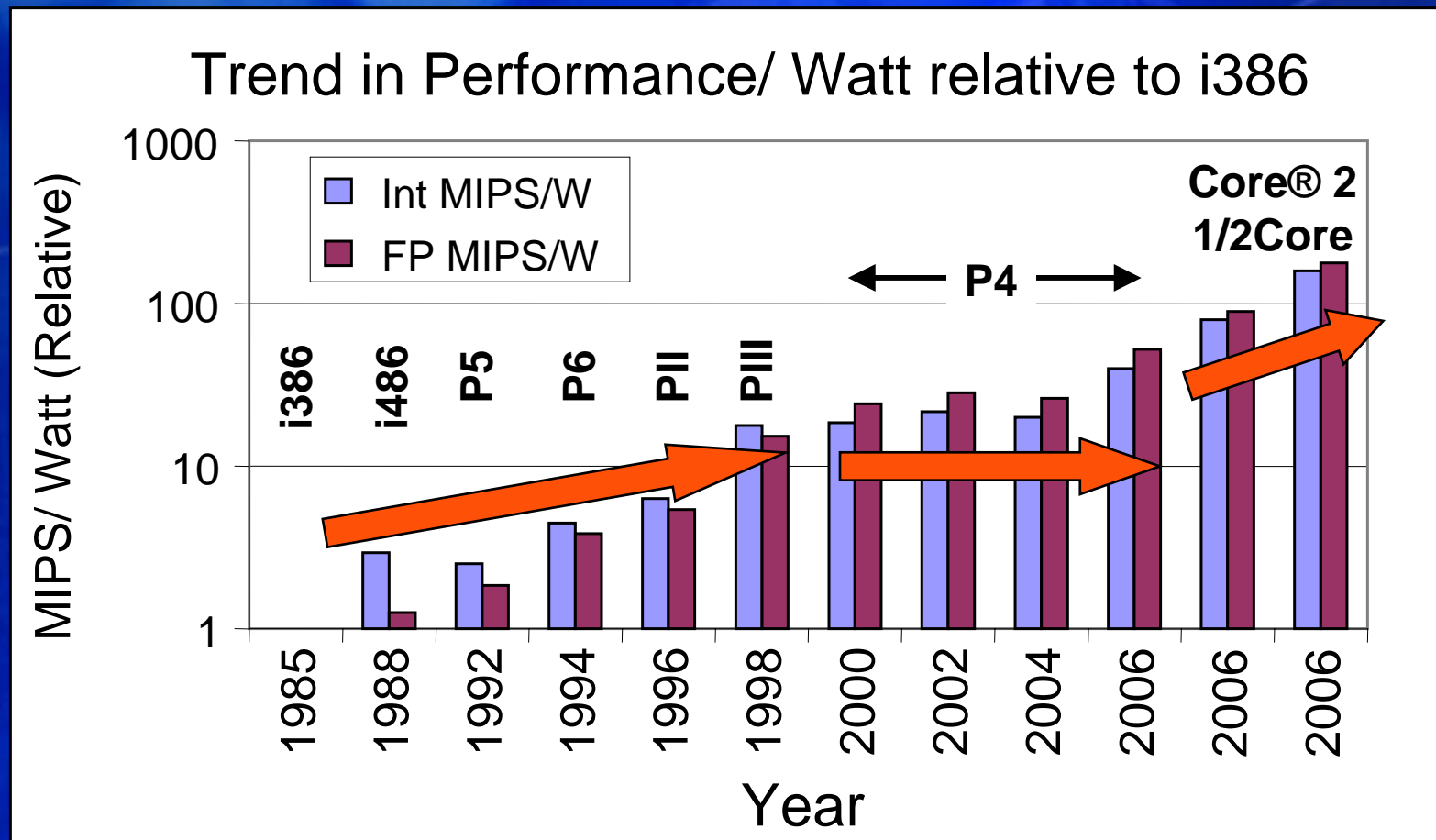
Performance/ watt improvement for both
integer and Floating point

Lead in 45nm Technology and Products
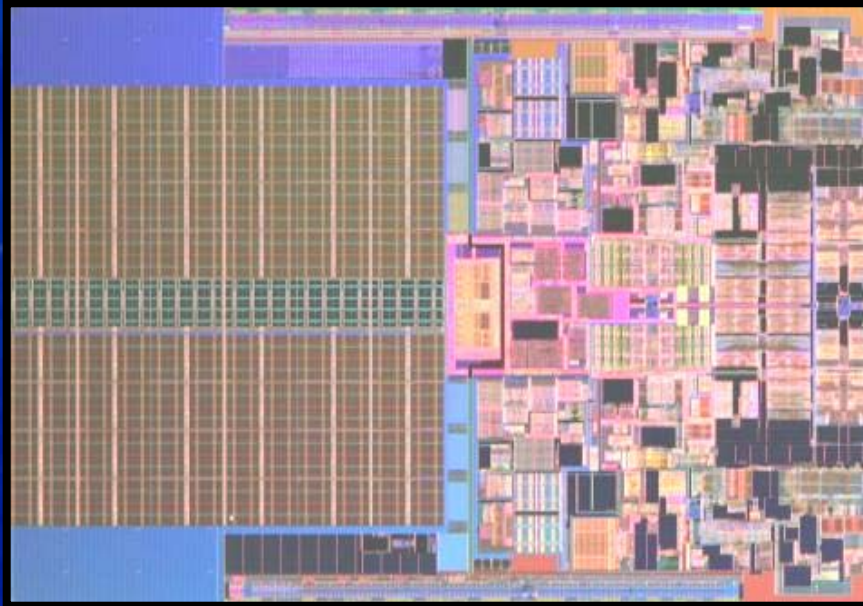
Intel® Penryn

Core™2 family processor

410/820 M transistors (2C/4C)

World's first working 45 nm CPU
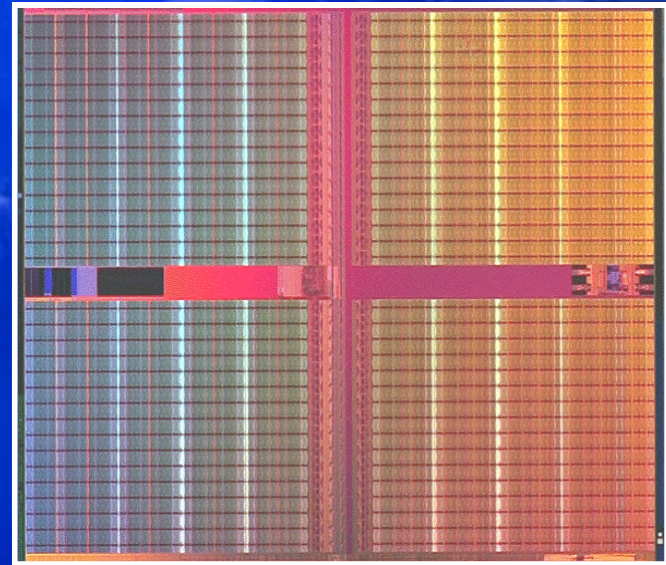
153 Mbit SRAM

0.346 μm^2 cell

119 mm2 chip size

>1B transistors

Functional in Jan 2006

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45 nm Yield Improvement Trend

Defect density (log scale)

0.13 um   90 nm   65 nm   45 nm

2000 2001 2002 2003 2004 2005 2006 2007 2008
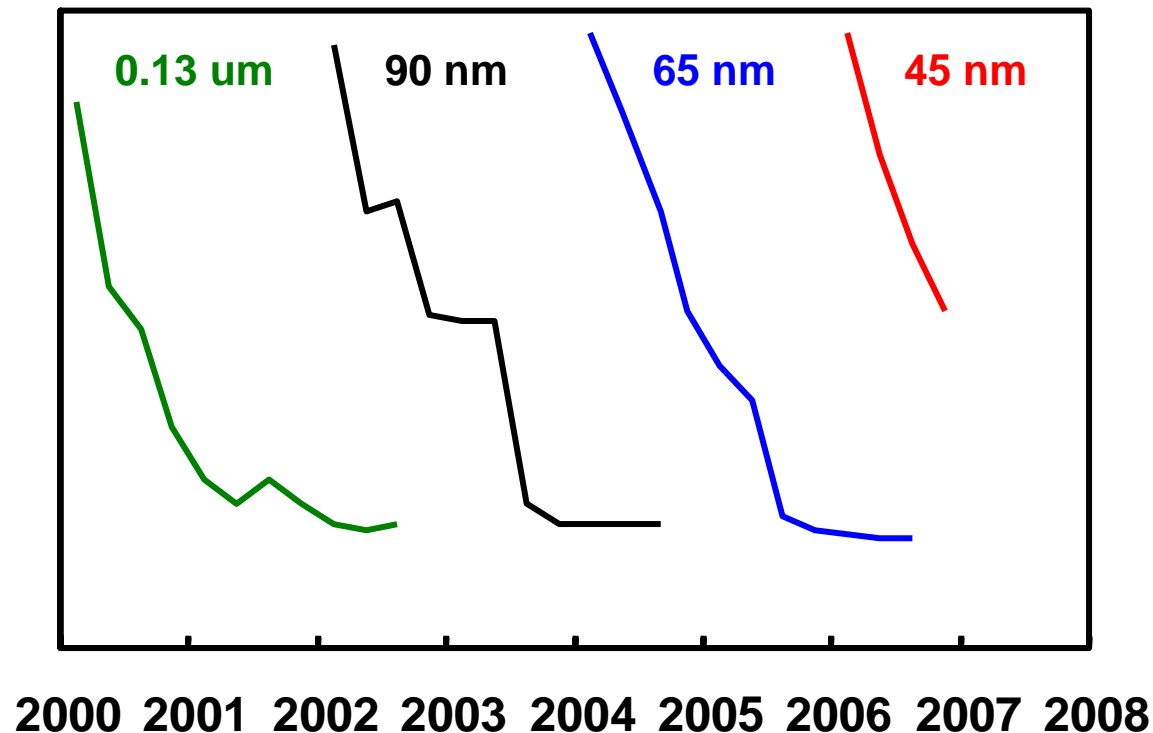
Excellent Yield learning and good reliability too

On track for production ramp in 2H '07

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SRAM Cell Size Trend

100

10

Cell Area
(um²)

1

0.5x every
2 years

0.1

1992 1994 1996 1998 2000 2002 2004 2006 2008

45nm 6-transistor
SRAM
cell area of 0.346 mm2

M. Bohr
Intel
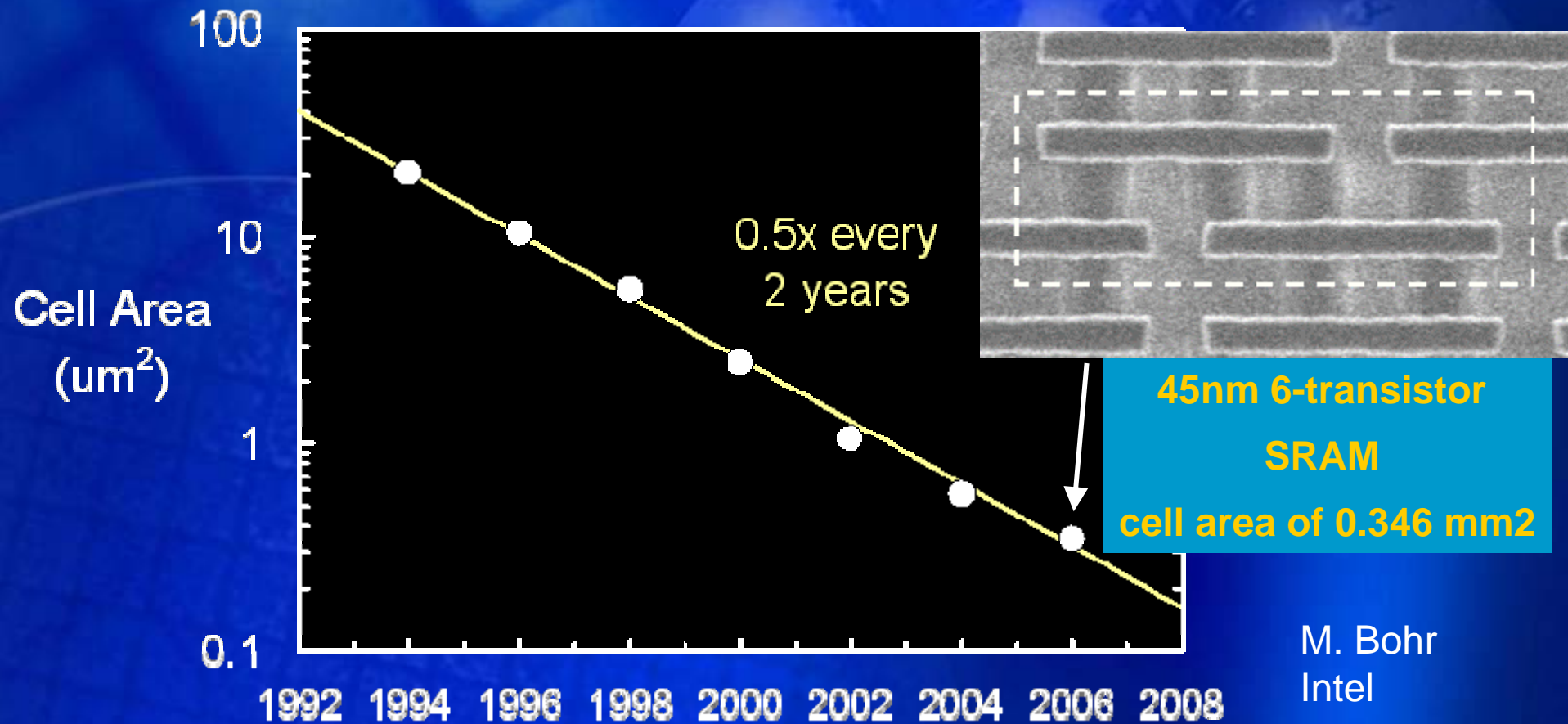
The trend continues

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High-k + Metal Gate Transistors

- ✓ **Integrated 45 nm CMOS process**

- ✓ **High performance**

- ✓ **Low leakage**

- ✓ **Meets reliability requirements**

- ✓ **Manufacturable in high volume**
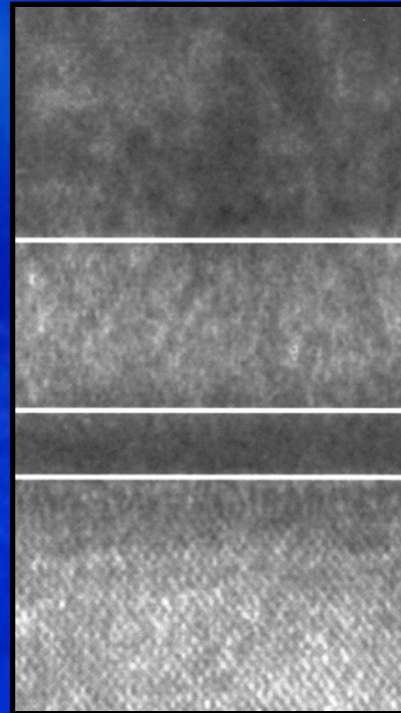
Low Resistance Layer

Work Function Metal
Different for NMOS and PMOS

High-k Dielectric
Hafnium based

Silicon Substrate

	High-k vs. SiO$_2$	Benefit
Capacitance	60% greater	Faster transistors
Gate Leakage	>100x reduction	Cooler chips

Gate Leakage scaling

Gate leakage A/cm2) — Gate leakage A/cm2)
Electrical Tox (nm)
SiO2
HK

Very High Innovation Rate

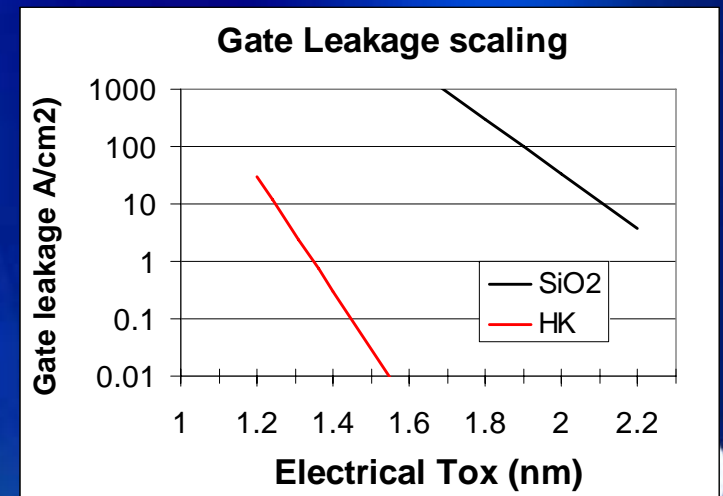| Materials | HighK-MG Xtors for performance & Low Power |
	LowK ILDs for interconnect
	Novel materials for strain and electrical Pformance
Transistor Architecture	Novel transistor architectures for HighK-MG
	TriGate Xtors and III-V integration in the future
Chip Architecture	Efficient Performance/Power with CoreTM2 MultiCore
	Monolythic integration of Graphics, Mem. Controller etc.
Platform Integration	Power & form factor optimization

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Many Reliability Challenges

- Increased Electric Fields
- The shrinking V_{max}-V_{min} window
- The development of robust High K/ Metal Gate transistors
- Dimensional scaling of interconnects and their liners
- Thermo-Mechanical limitations of very LowK ILDs
- Soft Errors
- Defectivity with scaled technology
- Transient and intermittent errors
- Fault tolerance

Innovation needed more than ever

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Gate Dielectric Field Trend

Gate Dielectric Electric Field
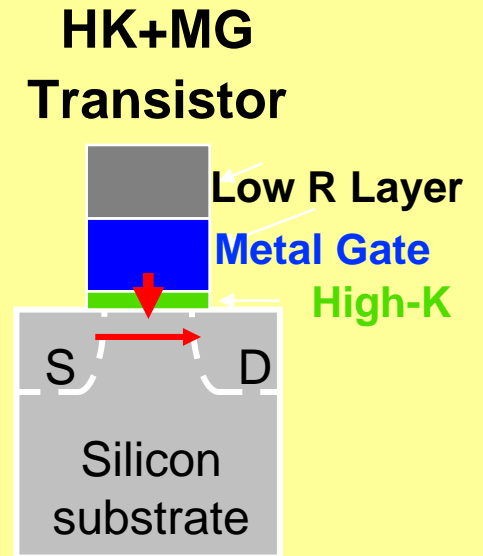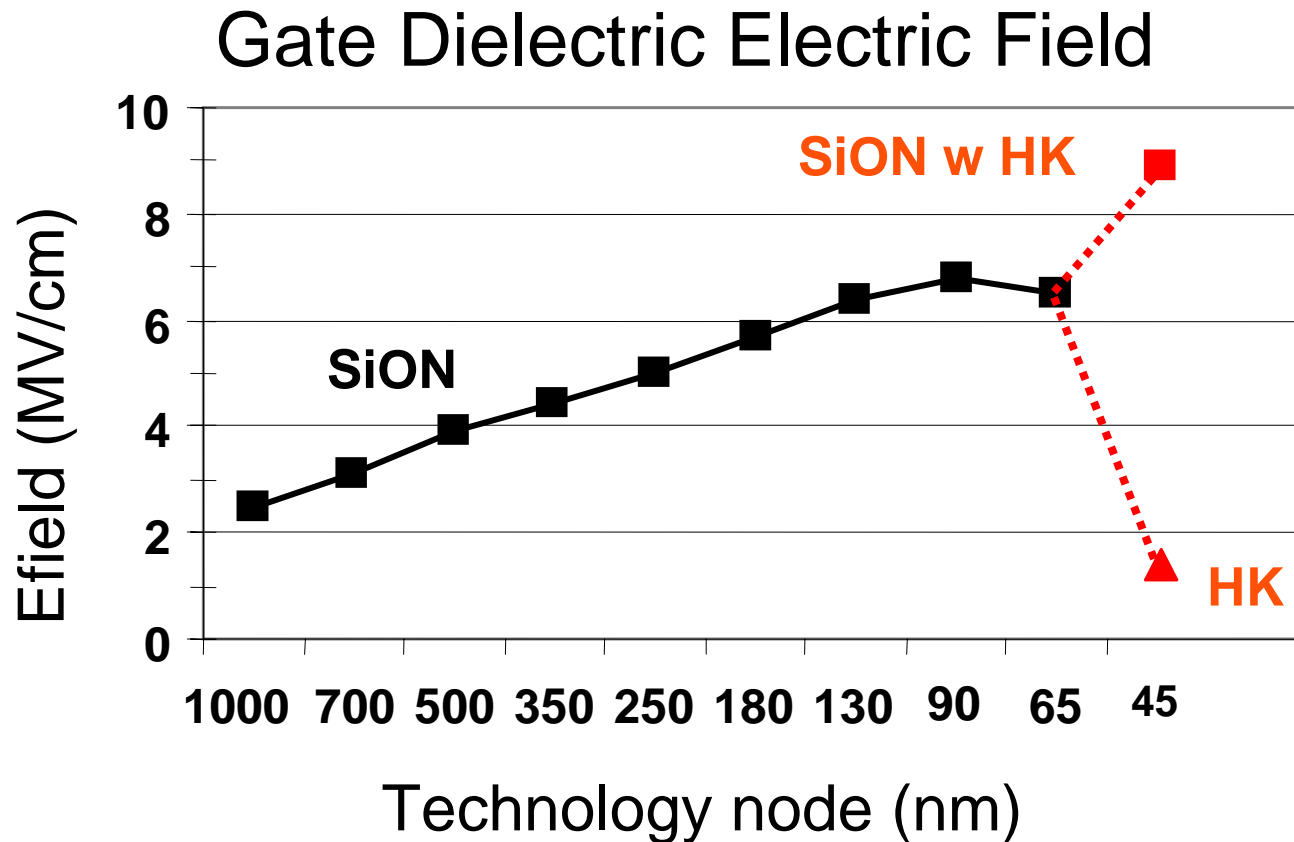
HK+MG Transistor

Substantial increases in Efield enabled by HK/MG

V_{max}-V_{min} window challenge

Vmax-Vmin trend
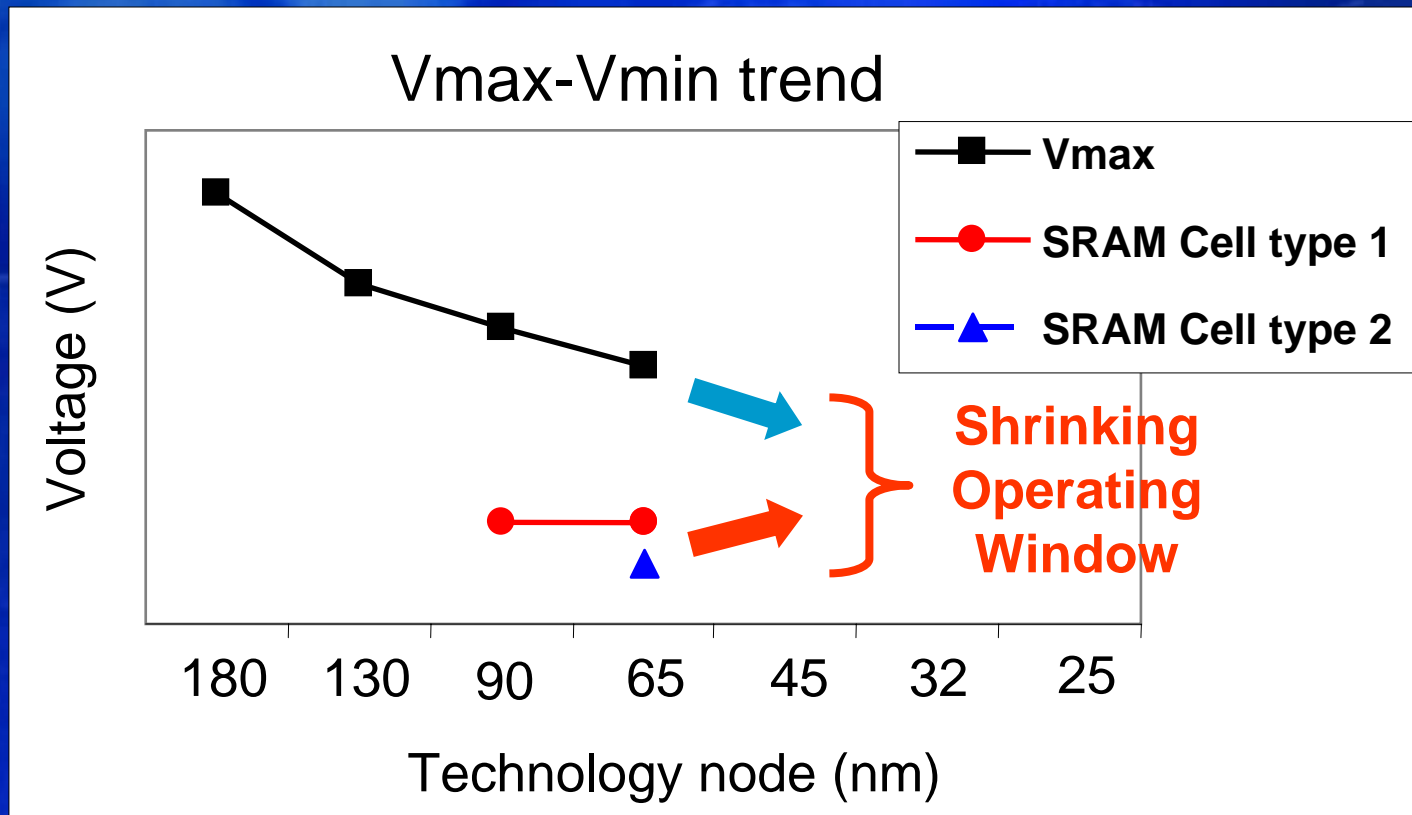
V_{max} ⬇ :Scailing for density, performance & power

V_{min} ⬆ :Transistor variability & increase bit count

Transistor variability impacts Vmin
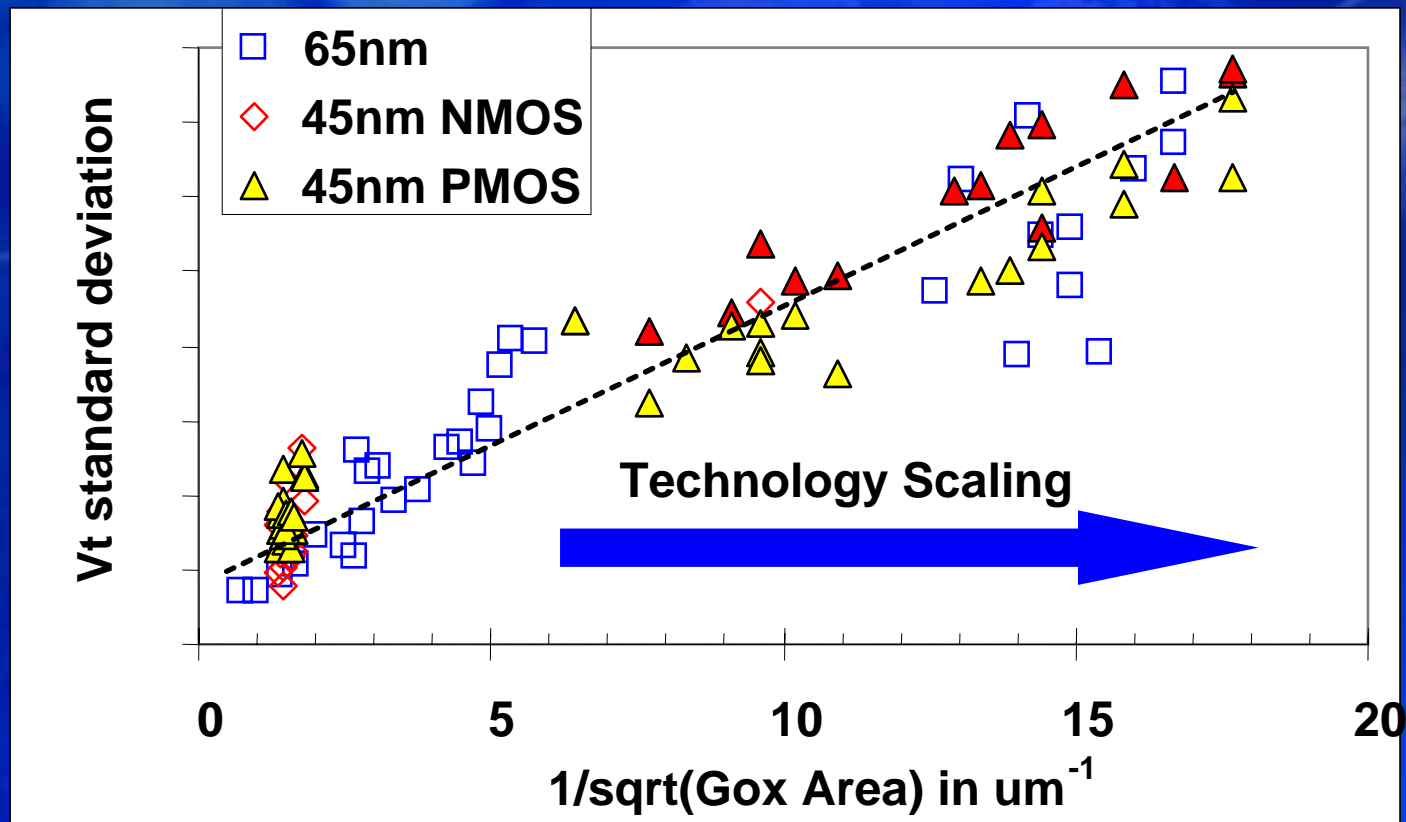
- Due to random dopant fluctuation and other process parameters
- Develop design techniques that can handle variability

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V_{min} impacted by bit count

Defective bits vs Voltage
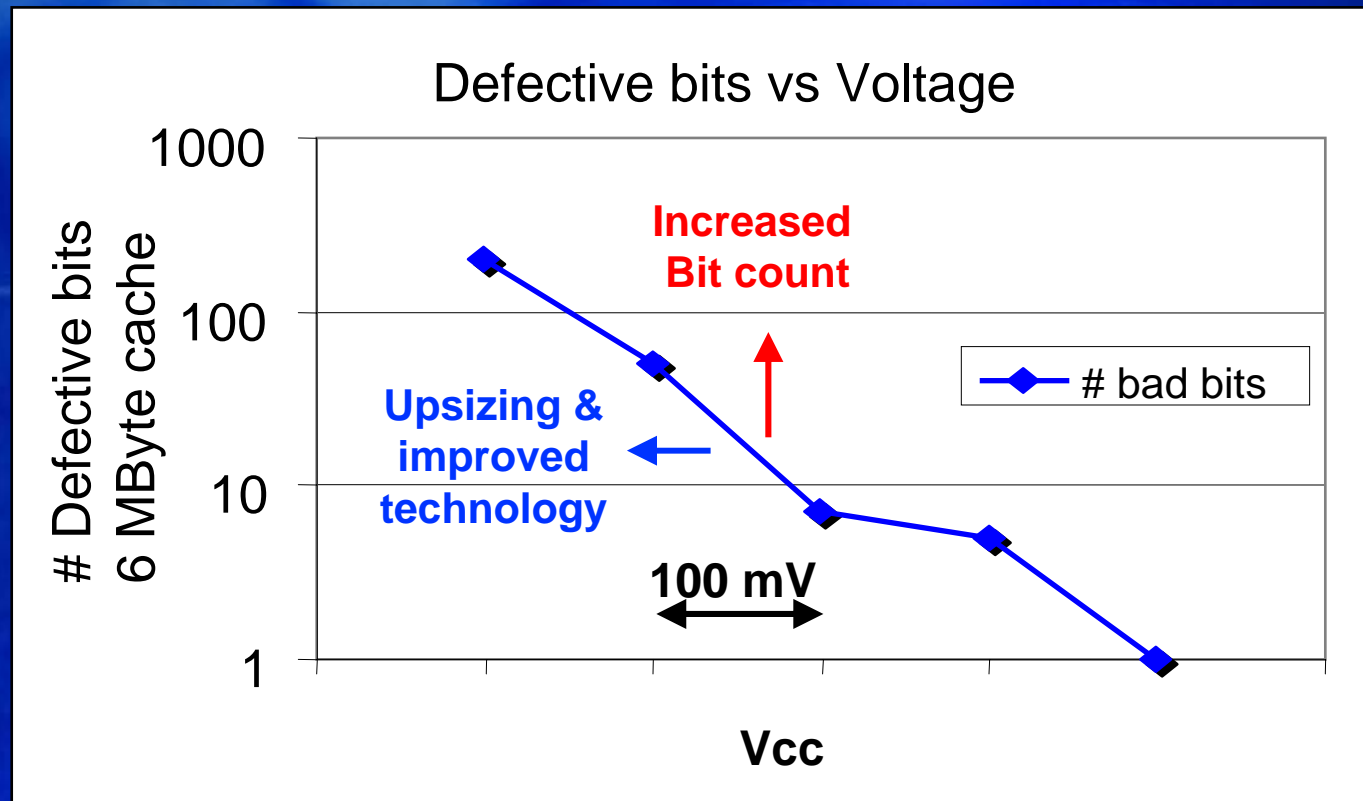
- Impacted by variability and defectivity
- Improved process and cell upsizing helps

Need Robust manufacturing process now and Fault Tolerance techniques in the future

Transistor degrades during use
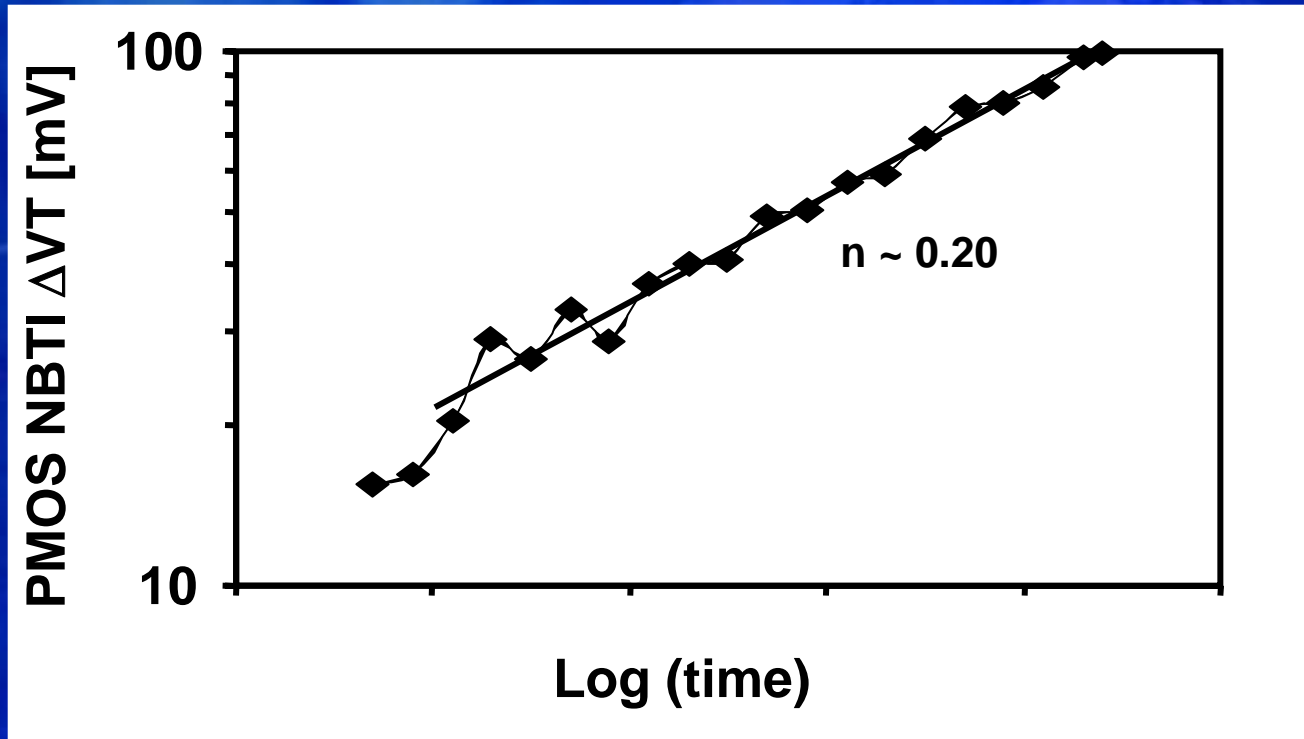
- Slow but continuous process
- Addressed by variation tolerant design and Frequency Guardbands at test

... and so does Product operating frequency

Fmax degradation in Burn-in
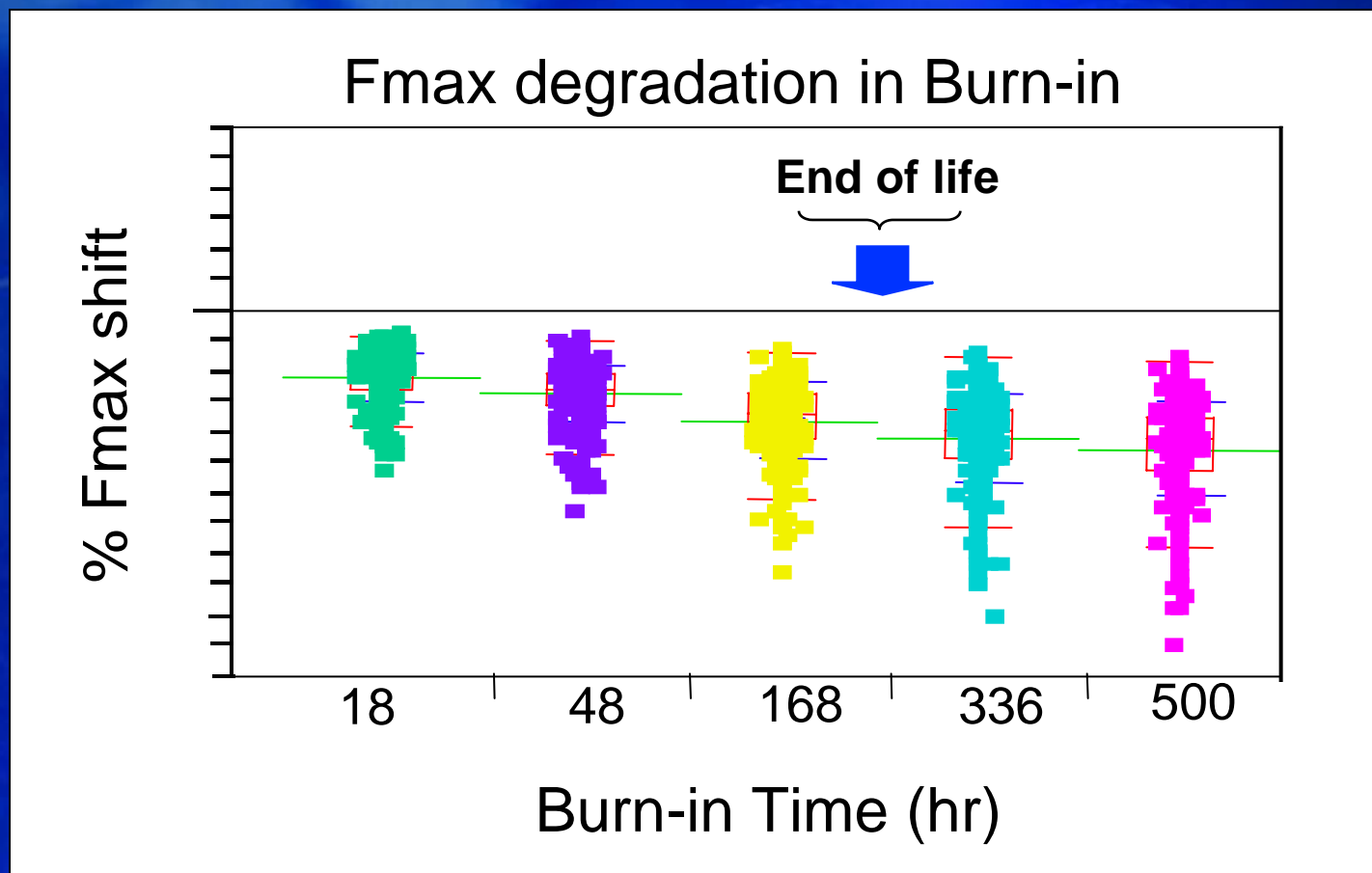
Test Guardbands used to eliminate customer impact

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Transistor degradation

PMOS NBTI degradation

Efield increases with scaling →

Process improvements ↓

Vt-shift [-mV]

80 · 60 · 40 · 20 · 0
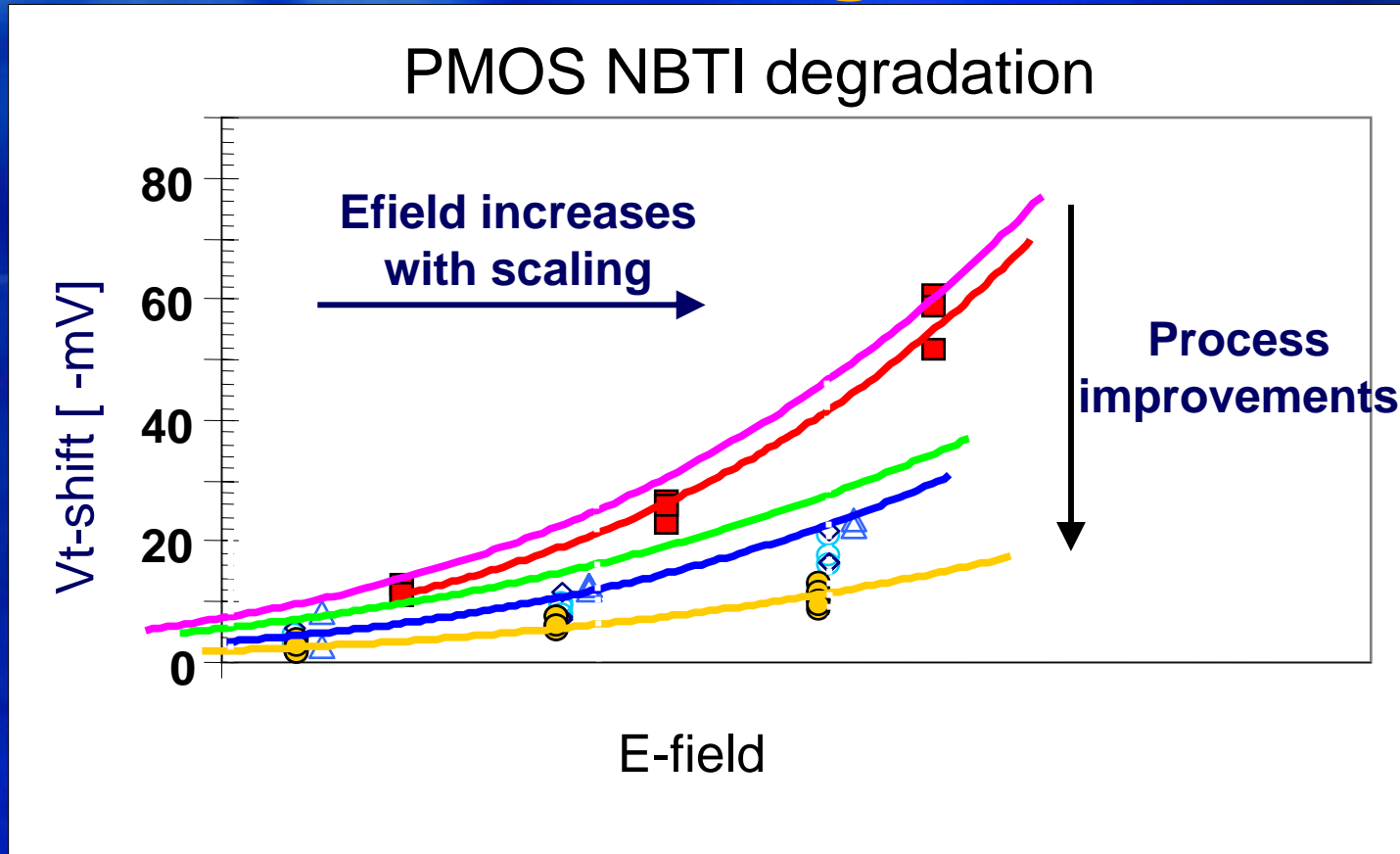
E-field

Process improvements are a must to counter the effect of increased E fields

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Transistor architecture & materials are changing

- ● Many new materials
  - – HighK/Metal Gates for gate leakage control and performance scaling ➔ Integration and reliability challenges
  - – Low K ILDs ➔ Thermomechanical risk may slow their introduction
  - – Lead free Bumps

- ● Clever changes in planar transistors
  - – Strain, epiaxial Source/ Drain layers

- ● Novel Transistor architectures like tri-gate

- ● Exotic options explored: from Carbon Nanotubes and semiconductor nanowires to III-V compounds

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Tri-Gate Transistors

Source   Gate   Drain   Gate Oxide

Source   Drain
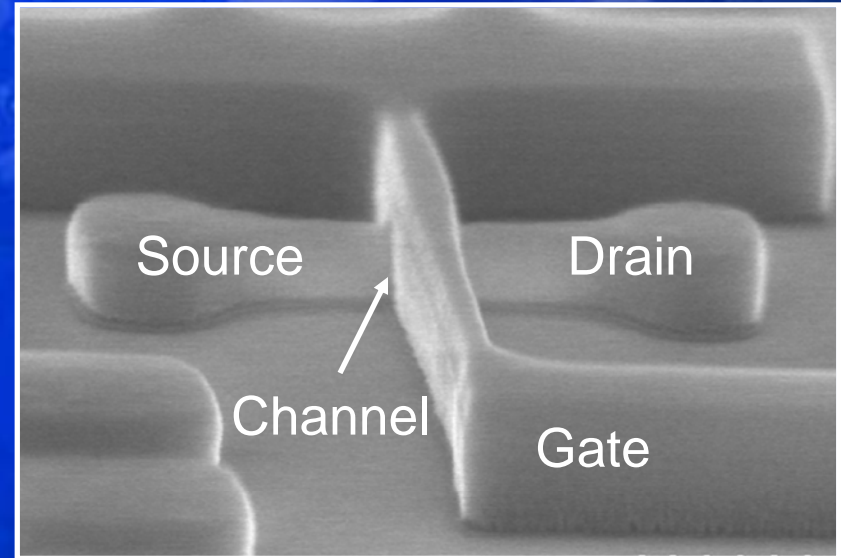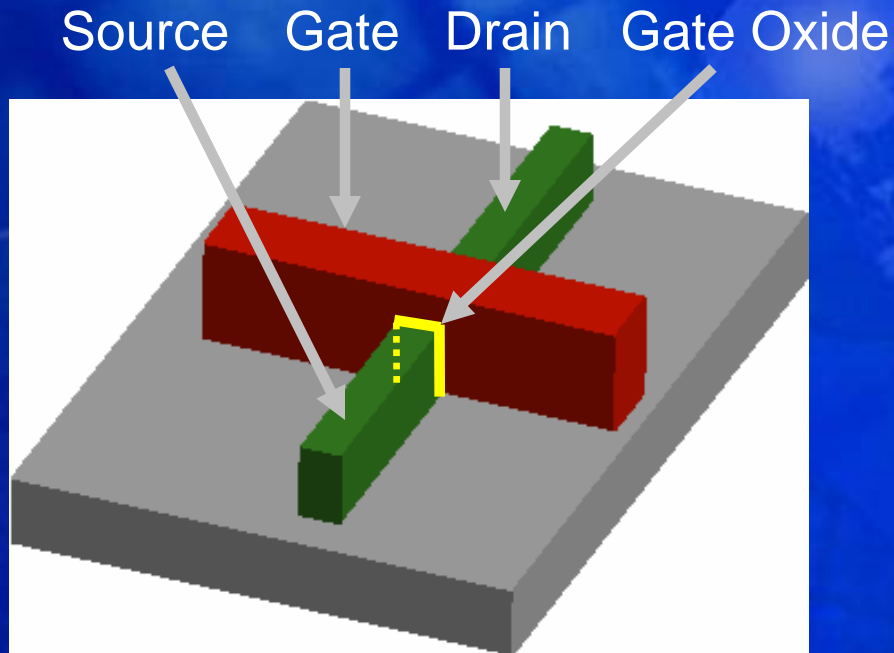
Channel
          Gate

- Transistor gate wraps around 3 sides of Si channel (Tri-Gate)

- Transistor channel is "fully depleted", unlike normal bulk CMOS

- Fully depleted operation reduces leakage current by up to 10x

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Increasing Electron Mobility

n-Mobility	Compound Semiconductors		
Si	GaAs	InAs	InSb
1	8	33	50

Increased electron mobility leads to higher performance and less energy consumption

- The challenge is integrating them with Silicon and improving Hole mobility

Scaling of the interconnect

Cu Resistivity vs Line Width

ohm-µm

Copper CD (um)

0.05 0.15 0.25 0.35 0.45 0.55 0.65

Source:Intel

65nm
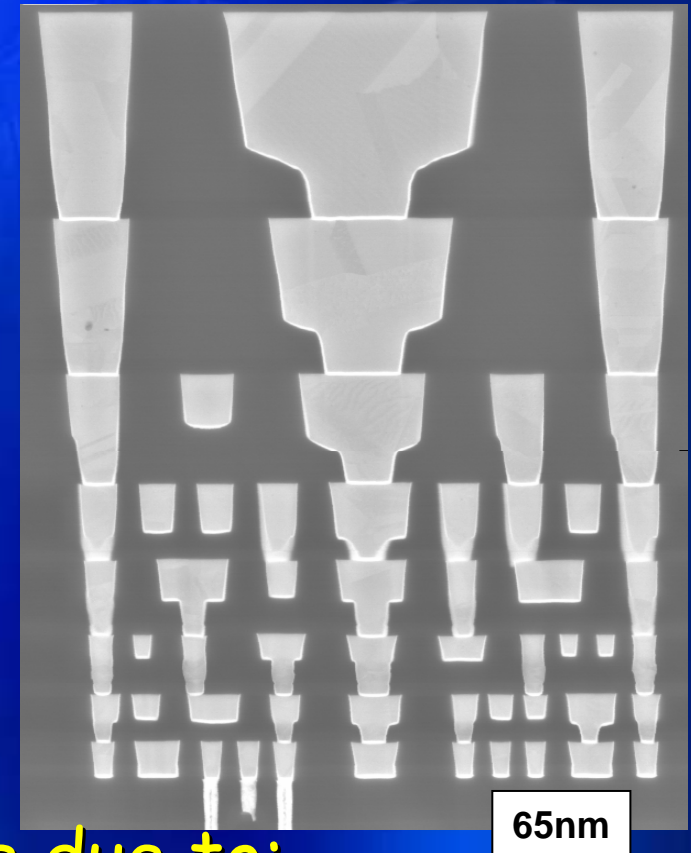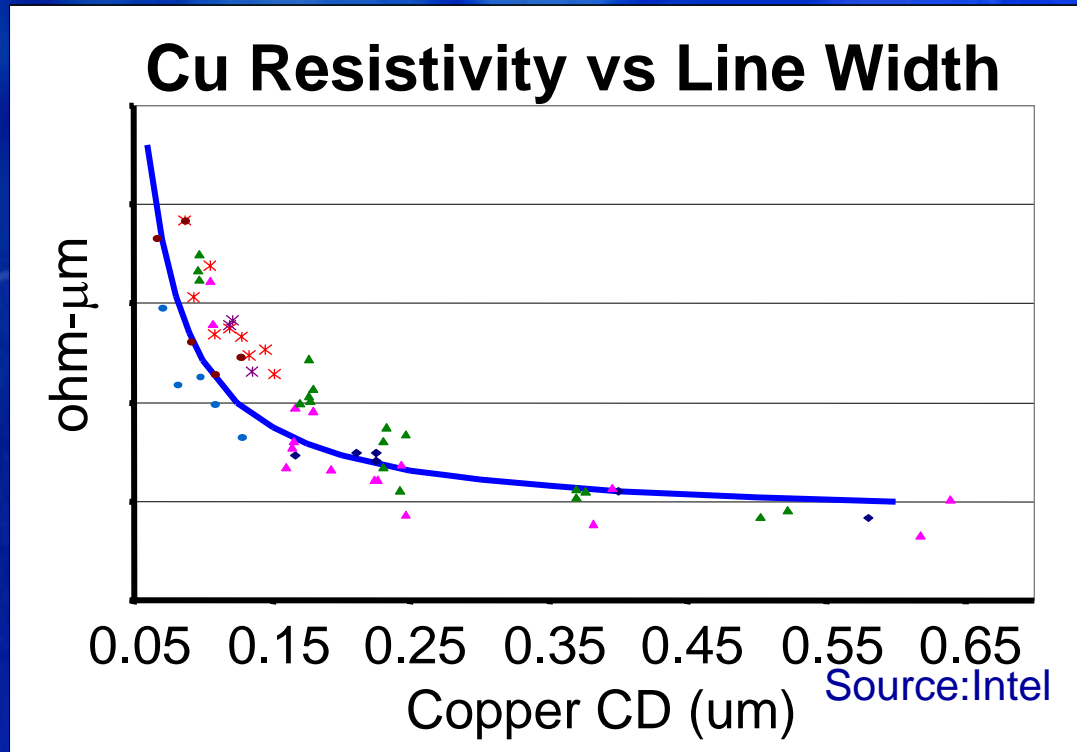
● **Effective resistivity increase due to:**

– Cross section reduction due to barriers

– Increased scattering from grain boundaries and surfaces

Tough but manageable challenges

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Single Event Upsets

- Transient errors that corrupt data but do not produce permanent damage (on limited doses)
  - Charge burst that overwhelms a storage node
- α particles in materials and atmospheric neutrons in terrestrial systems
- Cosmic rays and heavy nuclei in space
  - Orders of magnitude higher fluxes than at sea level
- This is just one class of transient errors
  - Others are noise related fails in the interconnect fabric etc.

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Single Event Upsets: Cache cell

Cache Cell SEU Trend

Legend: α FIT, n FIT Terrestrial, Total FIT

X-axis: Technology (nm) — 180, 130, 90, 65, 45
Y-axis: SEU/ Bit (a.u) — 0, 5, 10
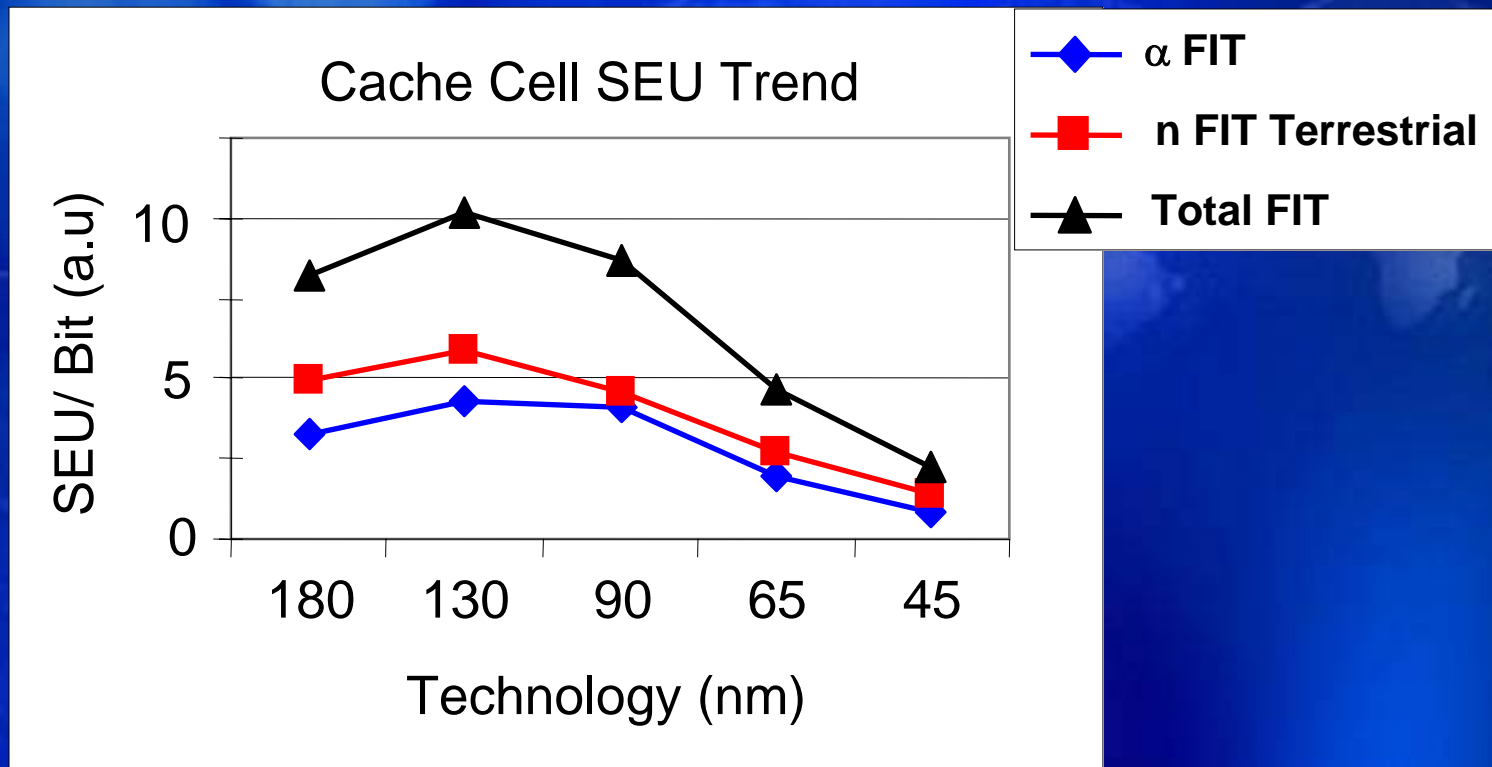
- SEU errors due to neutrons from cosmic rays and α particles from residual impurities
- Reduction in charge collection dominates over reduction in critical charge

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Single event upsets: Multi-bit fails
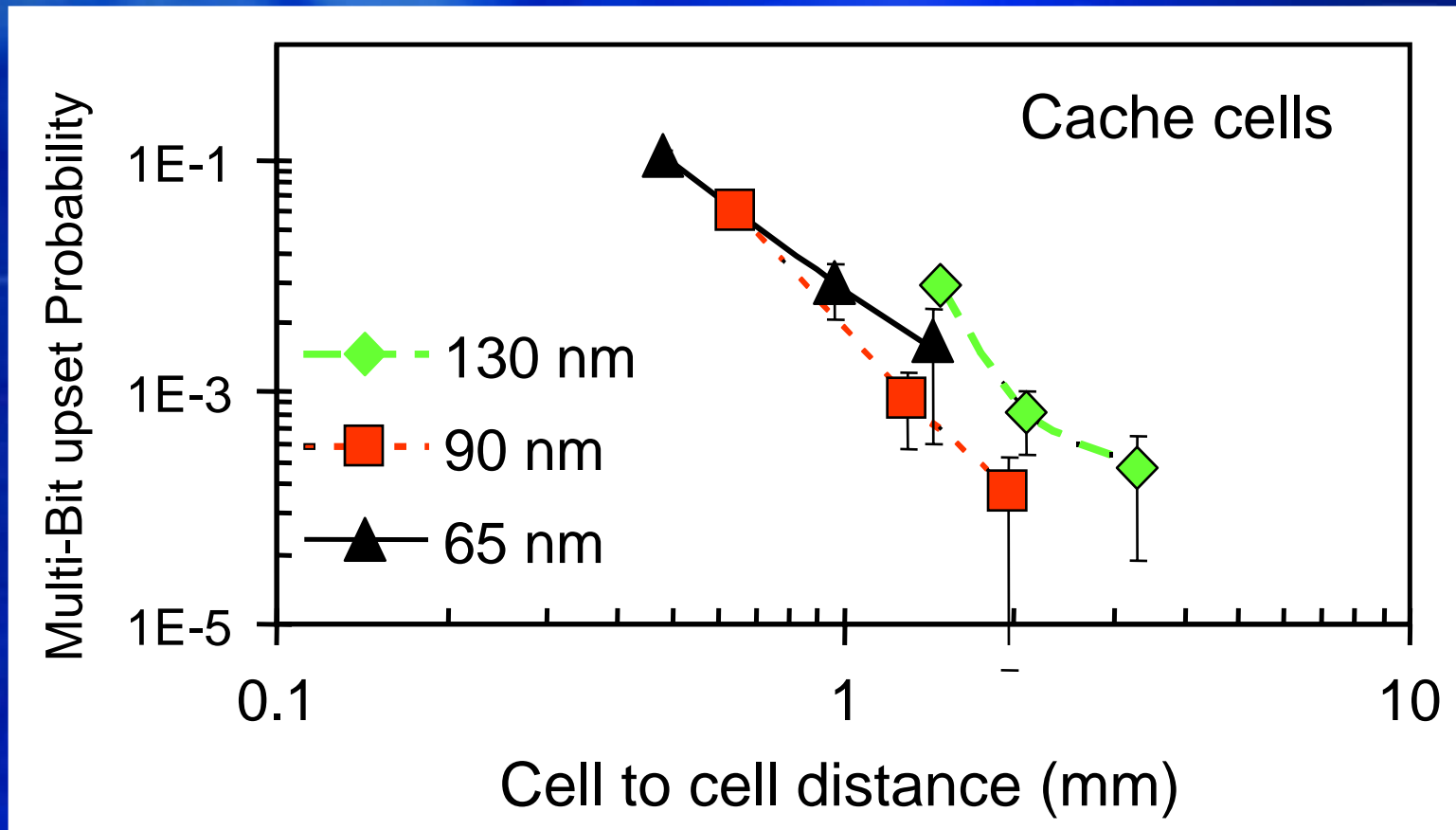
- Multi-bit errors are increasing as a proportion of fails
- Expected consequence of increased charge sharing

Single Event Upsets: Logic latches
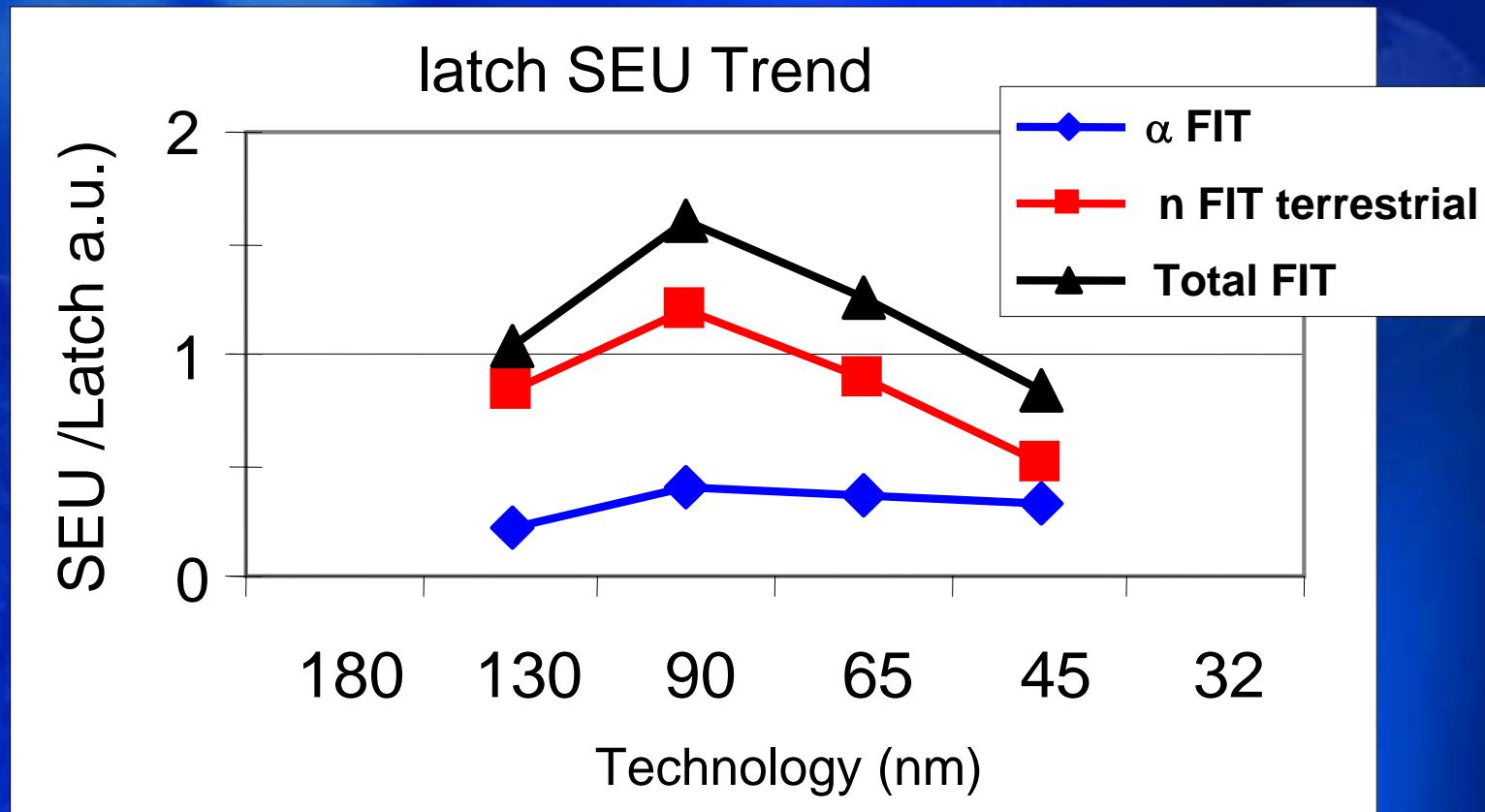
- Similar trend starting for latches
- 45 nm results still preliminary

Single Event Upset: Chip impact

SEU Trend

10 — (SEU Norm to 130nm)

2X increase in RAM cell & latch count per generation

logic

Add features to reduce error rates

cache arrays

1 —

180 130 90 65 45 32

Technology (nm)
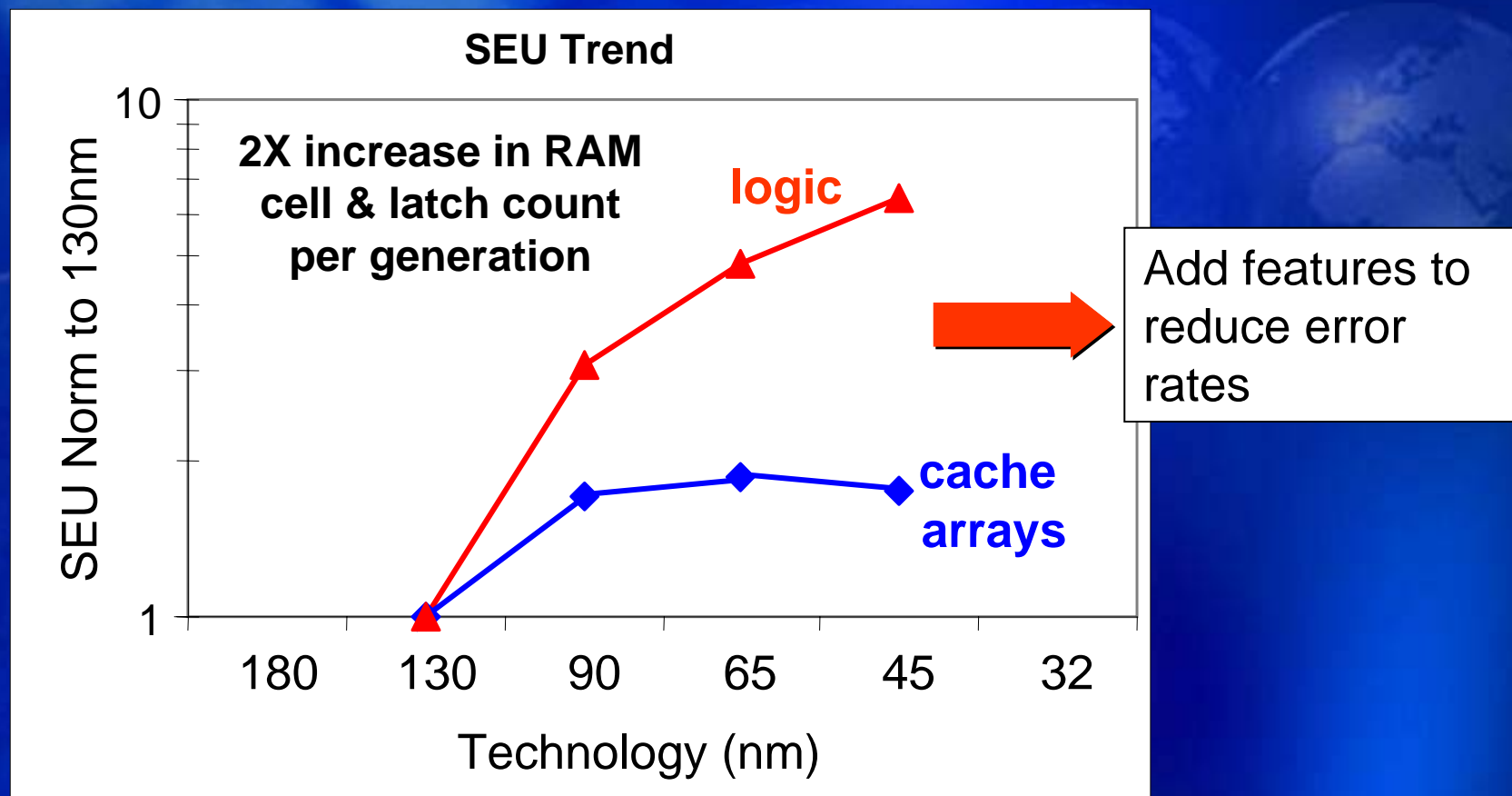
- Saturation for cache arrays
- Getting there for logic. Perhaps in 32nm

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Circuit contributions to SEU in a typical microprocessor

Static combinational logic

Residual Unprotected memory

Flip-flops

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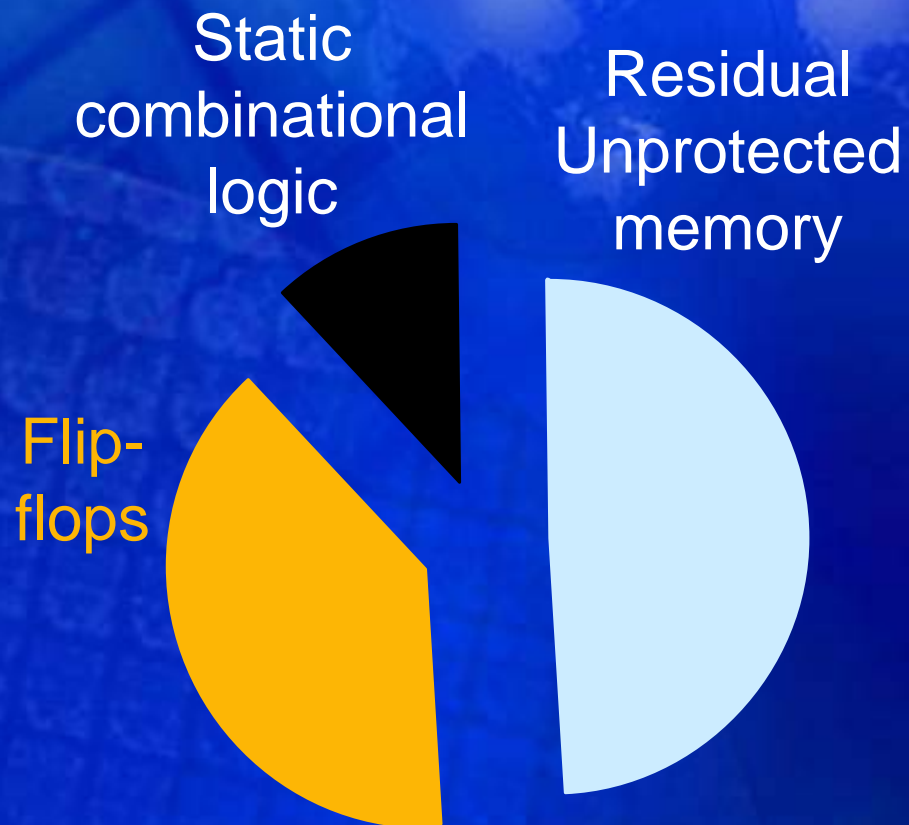
Many protection options proposed

- Adding Parity/ ECC to logic arrays and Register Files
- Replication of functional units or cores
- Lock-step for cores or complete chips
- Residue Checking
- Redundant multithreading
- Fingerprinting
- Modified Scan latches
- Hardening of worst contributing latches

What is the goal that we are trying to meet?
What is the value proposition for HPC?

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Recap of fail types & trends

Fail type	Trend	Solution space
Hard Fails	Flat	• Continued Process improvements • Architectural fault tolerance(2)
Parametric degradation	Increasing	• Continued Process improvements • Guard-bands • Architectural fault tolerance
Intermittent	??	• Continued process improvement • Architectural fault tolerance(2)
Transient (noise)	Increasing	• Continued Process improvements • Guard-bands • Architectural fault tolerance (1)
Transient (Ionizing Rad)	Increasing to flat	• Improved estimation methodology • Hardening of critical elements • Architectural fault tolerance (1)

(1) **Such as EDAC: (local circuit, component or system level)**

(2) **Requires self-diagnostics and redundancy**

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Fault Tolerance trends/ needs

- Conservatism in technology to eliminate errors to Many Sigma will cut into performance

- Fault Tolerant schemes will allow few errors to occur by providing the means to detect and correct
  - Minimal to no impact to the customer

- The continuation of Moore's Law makes transistor availability plentiful and enables a much broader thinking in Fault Tolerance
  - Local Circuit and functional circuit block level
  - Multi/ Mary core availability
  - Complement hardware /chip strategies with Platform system strategies

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Help needed from HPC experts

- What are the RAS Requirements for various categories and uses of HPC?
  - Are there agreed targets that can guide us?
  - Can a $ value be assigned to them?

- How can System architecture and Software help and complement the effort at the component level?

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  - Many new device types and materials
  - A challenge as well as an opportunity

- **High RAS will require global fault management strategies along with robust circuit design**
  - Better understanding needed on RAS requirements
  - Research and Cost effectiveness of proposed options

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