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THE DIAGNOSTICS' BACK END SYSTEM BASED ON THE IN HOUSE DEVELOPED A|DA| AND A|D|O BOARDS

A. O. Borga#, R. De Monte, M. Ferianis, L. Pavlovic, M. Predonzani, ELETTRA, Trieste, Italy

Abstract

Several diagnostic instruments for the FERMI@Elettra FEL, among them the Bunch Arrival Monitor (BAM) [1] and the Cavity Beam Position Monitor (C-BPM), require accurate readout, processing, and control electronics integrated within the main machine control system. The back end platform, based on the MicroTCA standard [2], provides a robust environment for accommodating such electronics, including reliable infrastructure features. Two types of Advanced Mezzanine Cards (AMC) had been developed in-house and manufactured for meeting the demanding performance requirements. The first is a fast (160 MSps) and high-resolution (16 bits) Analog to Digital and Digital to Analog (A|D|A) Convert Board, hosting 2 A-D and 2 D-A converters controlled by a large FPGA (Virtex-5). The FPGA is also responsible for service and host interface handling. The latter board is Analog to Digital Only (A|D|O) Converter, derived from the A|D|A, with an analog front side stage made of four A-D converters. The overall systems' architectures, together with the specific AMCs' functionalities, are described. Results on performance measurements are also presented.

BACK END OVERVIEW

Figure 1 shows a block diagram of the general architecture of the high-bandwidth, real-time diagnostics back end. Three sub-systems can be identified according to their installation location:

Tunnel area: hosting the *monitors* and the monitors' *front-end electronics* responsible for signal pick-up, conditioning, and transmission to the back-end.

Service area: *back-end* and *A|D|A* and *A|D|O boards*, the system fulcrum where further signal conditioning, data processing, analysis, and computations are performed before data are sent back to users in the control room.

Control room: the users' control and monitor Linux/Tango PC, for data storage, further off-line analysis, and visualization.

The sub-systems are interfaced through transmission media chosen according to the different sections' specific needs. From the tunnel area to the service area the **A-B interface** carries signals via shielded coaxial or optical cables, for noise immunity. The cabling of the A-B interface is a task left to the monitors and front-end designers. The **E-F interface** connects the back-end crates to the control room's PC through standard Ethernet CAT6 cables and doesn't require particular attention. In the service area inside the back-end system, flexibility is more of a concern, so boards are connected through the **C-D interface** with SMA coaxial cables (for analog signals) or flat ribbon cables (in the case of digital signals).

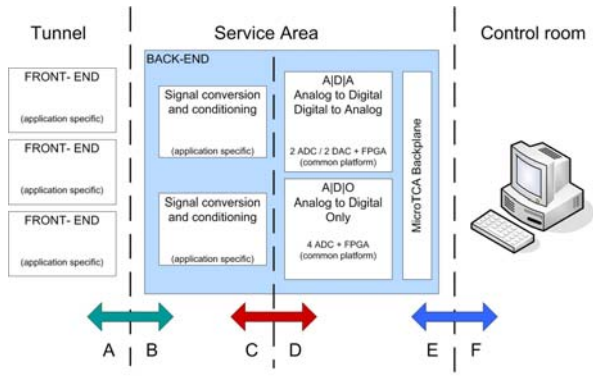

Figure 1: Block diagram of a diagnostic system based on µTCA and A|D|A and A|D|O AMCs

The C-D interface inside the back-end system's crate is used to interface three types of modules:

A|D|A and A|D|O AMCs: Advanced Mezzanine Cards (AMCs) for digital processing; FPGA based.

Custom Passive AMCs: interface transition cards that adapt front-end signals to the inputs of A|D|A and A|D|O.

Custom Active AMCs: standalone modules, for application-specific tasks not strictly related to diagnostics, that might not require an interface with A|D|A or A|D|O (e.g. timing and trigger cards, storage devices, processor cards, etc).

The whole electronics is based on the Micro Telecommunications Computing Architecture, which is beyond the scope of this paper but is described in, for example, [2]. For the C-BPM diagnostics case a 3D mock-up of a hypothetical system is shown in Figure .

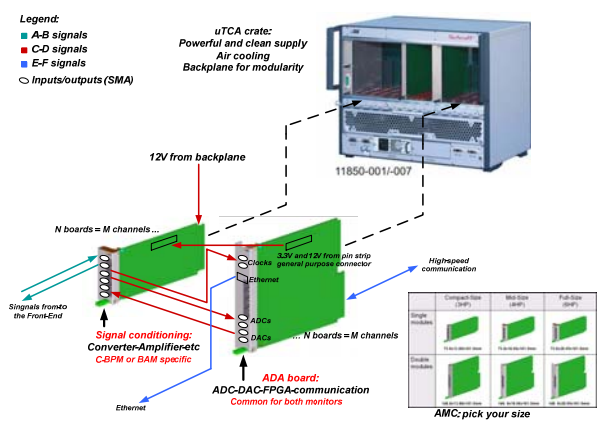

Figure 2: Example 3D mock-up of a system

A|D|A MODULE ARCHITECTURE

Block diagram

The main purpose of the Analog to Digital and Digital to Analog (A|D|A) [3] converter Advanced Mezzanine Card (AMC) is acquisition, processing, and generation of fast analog signals. The architecture is based on a large Xilinx Virtex-5 FPGA responsible for the data handling of all the external inputs, the data processing, and the interface to users. A block diagram of A|D|A is shown in Figure 3.

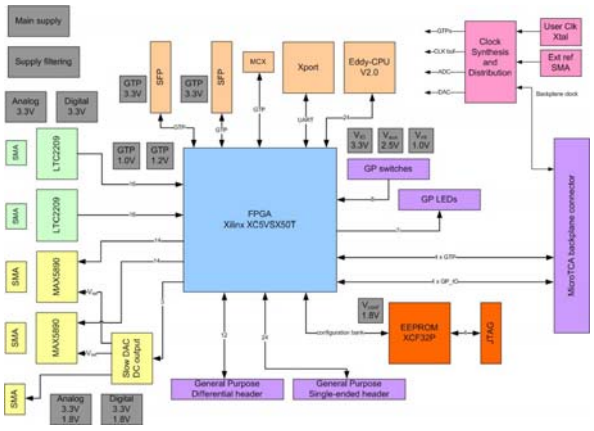

Figure 3: A|D|A AMC module block diagram

It has the following seven major subsystems:

1. **Power section:** from the backplane 12V all local voltages are derived by means of Point Of Load (POL) switching (for digital sections) and Low Drop Out (LDO, for analog sections).
2. **Clock distribution:** a programmable and configurable clock tree provides precise timing to on board devices with the freedom to choose between several internal or external references Figure 4.
3. **Configuration section:** the logic can be programmed with direct access through an onboard JTAG chain, or remotely via the backplane or via Ethernet.
4. **Analog inputs and outputs:**
   - 2 LTC2209 ADC inputs 160 Msps 16 bits, electrically isolated with Bandwidth 50 – 700 MHz of the input filter and Amplitude range V_{p-p} 2.5V
   - 2 MAX5890 DAC outputs 600 Msps 14 bits, AC coupled with Bandwidth 0.130 – 425 MHz of the output filter and Amplitude range V_{p-p} 1V
   - 1 LTC2602 dual DAC output 16 bits, DC coupled with Bandwidth DC – 1 KHz and Amplitude range 0 – +3.3 V
5. **Computational core:** the whole board's activity swings around a Xilinx Virtex-5 SX50T FPGA. All external signals to and from the board are directed to the logic device
6. **Remote access:** access to the logic is granted in several ways
   - *Lantronix*: 1Mbps Ethernet (TCP/IP or UDP/IP)
   - *Eddy-CPU:* 100Mbps Ethernet (TCP/IP or UDP/IP)
   - *Small Form-factor Pluggable (SFP) ser-des:* 1Gbps custom link based on ISO/OSI layer 0 and 1 from the Ethernet standard.
   - *uTCA Backplane via Gigabit Transceiver Pairs (GTPs):* 4 x 1Gbps custom protocol links
   - *uTCA Backplane via standard IOs:* 4 x 200Mbps custom protocol links
7. **General purpose inputs and outputs:** 24 single ended and 12 differential lines, directly interfaced to the FPGA, are available through two standard 1.27 mm pitch pin strip connectors for users' custom requirements. These connectors also provide +3.3V (500 mA) and +12V (1A) users supplies.

Clock distribution

A fully configurable and programmable clock tree is available onboard (Figure 4). The ADC (4.5 – 160 MHz) and DAC (4.5 – 600 MHz) stages can be independently supplied with external clock sources through SMA inputs on the front panel. The FPGA can be clocked off of the same external clock either from the DAC or ADC inputs; or timed independently from one of the onboard clock sources. Alternatively the whole board can be timed by high-accuracy (tens of pico-seconds range) frequency synthesizers starting from a low frequency (14 – 37.78 MHz). Frequency selection and tree setup are accomplished by setting jumpers. The backplane and other data transfer and communication sections (e.g. Gigabit links) are timed independently having other clocking requirements.

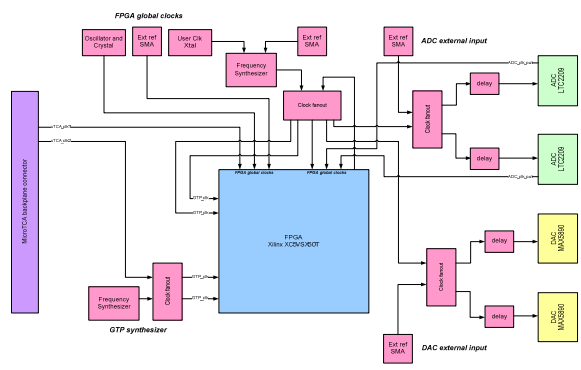

Figure 4: A|D|A Clock generation and distribution

Firmware top level diagram

The idea behind the firmware architecture depicted in Figure 5 is to provide black box core logic to support a **user's space** containing application specific algorithms. Three blocks can be then identified and developed separately: **control and monitoring**, **interface layer**, and **clock and timing**. The control and monitoring is a portion of the chip devoted to interfaces to/from the communication world, i.e. the Lantronix, the Eddy-CPU, and the backplane.

Data to the rest of the logic is stored inside a memory mapped RAM based area, providing a fully asynchronous, independent and well defined separation between different blocks.

The interface layer consists of a series of buffers controlled by state machines whose purpose is to collect and store the data to and from the ADCs and DACs. Their key role is then to absorb possible read/write delays and synchronize the readout to the internal logic's speed.

The clock and timing contains all the logic necessary for providing clocks to the different sections described above: it includes PLL, DLL, dividers, multipliers, etc.

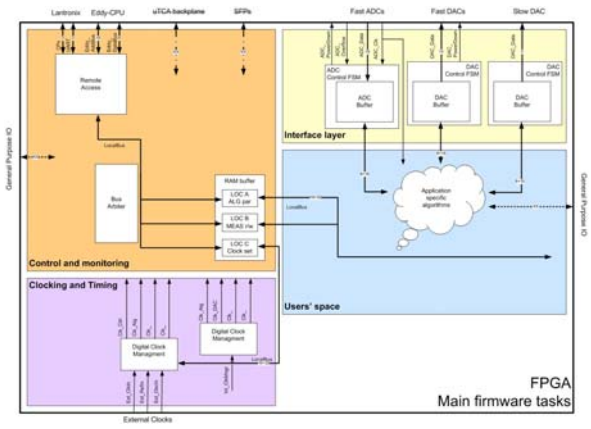

Figure 5: block diagram of the firmware sub-modules

A|D|O MODULE ARCHITECTURE

Block diagram

The Analog to Digital Only (A|D|O) converter Advanced Mezzanine Card (AMC) is derived directly from A|D|A. Like its predecessor, it is based on a large Xilinx Virtex-5 FPGA responsible for the data handling of all the external inputs, the data processing, and the interface to users. A block diagram of A|D|O is shown in Figure 6.

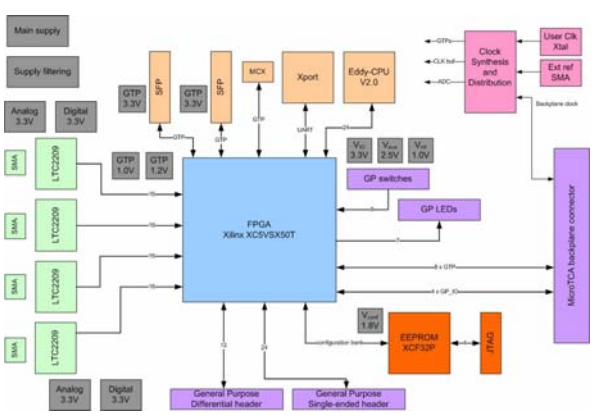

Figure 6: A|D|O AMC module block diagram

The main difference between the two cards is the front-end that in the A|D|O case in made of 4 A-D converters. The backplane connectivity had been enhanced and improved, as well as the clocking architecture.

Clock distribution

Based on the experience gained measuring with A|D|A new solutions for further adding flexibility to the clock distribution tree of A|D|O (Figure 4) had been adopted. The ADC (4.5 – 160 MHz) stage can still be independently supplied with an external clock source through SMA inputs on the front panel. The FPGA can run clocked off of the same external clock for the ADC inputs, as well as being timed independently. Providing more clock capabilities via the backplane allows future development of a dedicated uTCA timing card. Thus a small 3x3 cross point switch had been added in-between the backplane and the rest of the clocks. Still available on board are high-accuracy (tens of pico-seconds range) frequency synthesizers starting from a low frequency (14 – 37.78 MHz). Frequency and tree setup are accomplished by setting jumpers.

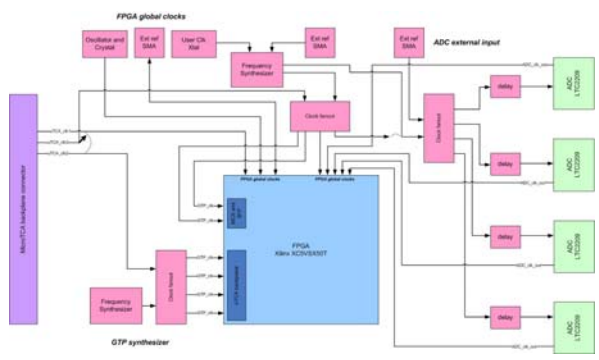

Figure 7: A|D|O Clock generation and distribution

Firmware top level diagram

As for most of the hardware design, the firmware architecture for A|D|O was ported from A|D|A. Tweaks for the light differences still need to be done, but the basic functions had been successfully ported from the previous card.

MEASUREMENTS ON A|D|A

Three main features of the board were identified as fundamental for guaranteeing the minimum board functioning:

1. Data generation through the DACs
2. Data acquisition through the ADCs
3. Remote access via the Lantronix XPort

DACs tests

Two types of periodic waves were synthesized using the two DACs present on the A|D|A board for testing the digital to analog conversion section. Results are shown in Figure 8 and Figure 9.

The first waveform was a plane sine wave at 60 MHz using a 120 MHz logic clock for the FPGA and a 240 MHz sampling clock for the DAC.

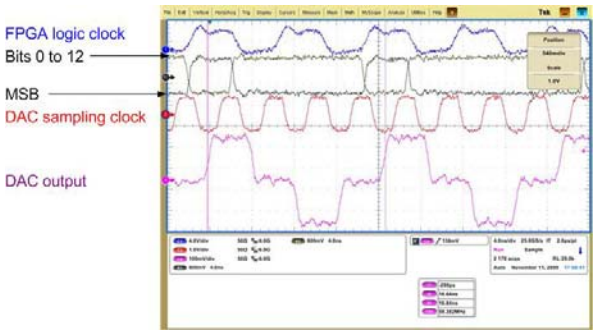

Figure 8: DAC synthesized pure sine at 60 MHz

The second waveform was a damped sine wave at 80 MHz using a 160 MHz logic clock for the FPGA and a 320 MHz sampling clock for the DAC.

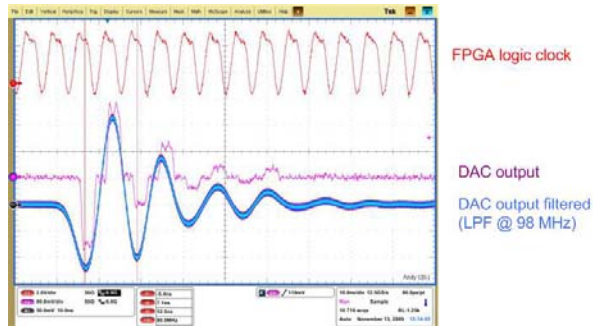

Figure 9: DAC synthesized damped sine at 80 MHz

ADCs tests

The ADCs were tested using two methods:

1. Loopback through the FPGA of the two inputs to the two DAC outputs.
2. Burst data transfer to a basic acquisition and display software

The results of the measurements are shown in Figure 10 through Figure 13. The sampling rate of the ADCs was set at their maximum (160 MHz). Though the DAC had been proven to run faster, the same frequency of the ADCs was chosen in order to avoid synchronicity issues.

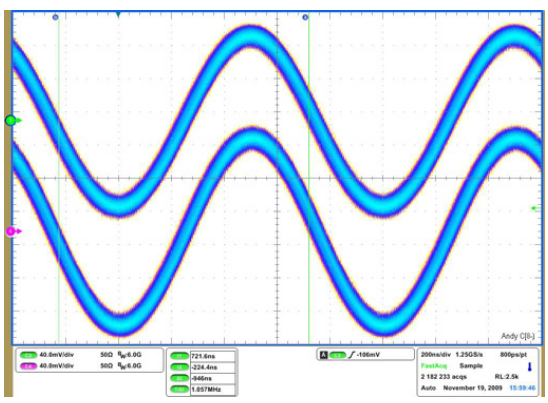

Figure 10: ADC1 and ADC2 acquisition of 1MHz sine wave redirected to DAC1 and DAC 2 outputs used as monitors

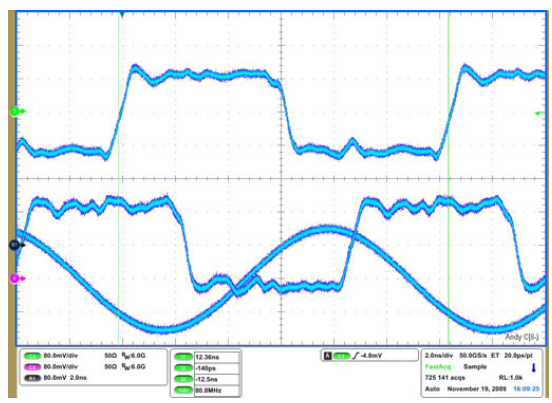

Figure 11: ADC1 and ADC2 acquisition of 80MHz sine wave redirected to DAC1 and DAC 2 outputs used as monitors

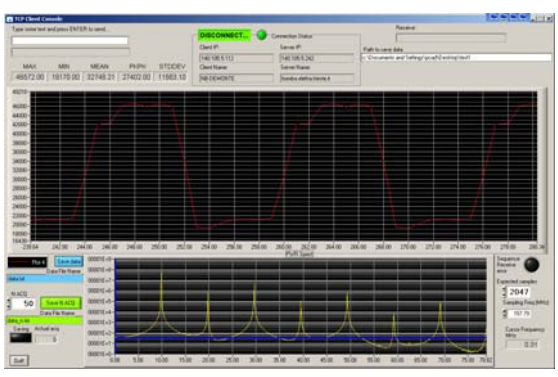

Figure 12: FFT on a 10MHz trapezoidal wave

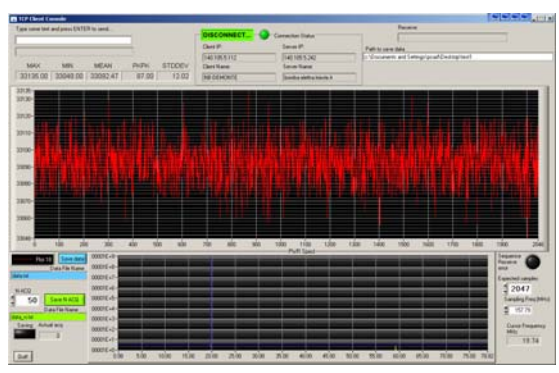

Figure 13: 34 values Std. Dev. on a 160MHz sine

Software communication interface

Several subsequent steps of software refinement led to the realization of a basic GUI, based on National Instruments' CVI, of fundamental utility for debugging. Capable of acquiring data from an open TCP/IP socket, it can either display them real time in both the time and frequency domain, as well as dumping acquisitions onto text files. A picture of the GUI is shown in Figure 12.

MEASUREMENTS ON A|D|O

ADCs tests

Data acquisition of one of the four ADC channels is shown below (Figure 14). All the other channels have equivalent performance on the whole range of frequencies tested 100 KHz to 160 MHz.

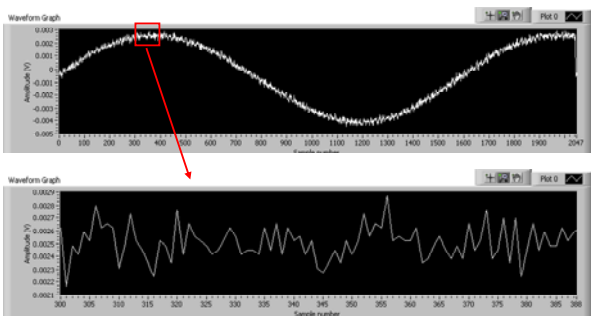

Figure 14: 700 µV noise on a 100 KHz 50 mV_{p-p} sine

As measured on the LTC2209 evaluation kit the noise of the input of the ADC is 5 LSB (Figure 15).

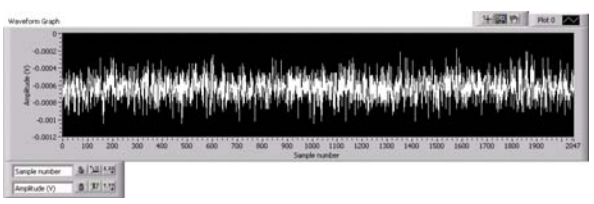

Figure 15: 5 LSB noise on 50Ω terminated input

Software communication interface

In order to debug at least the basic functionalities of the module, the analog front-end of the card with its four ADCs had been tested using the first control interface used for A|D|A: data stored in the ADC RAM buffer are transferred to the PC via ChipScope and the analyzed with a LabView GUI. Figure 14 and Figure 15 show the result of one acquisition with this technique.

DEVELOPMENT FRAMEWORK

The A|D|A project is a brave step toward an ambitious and far-seeing final goal: leading the road toward uTCA based systems at Elettra. Moreover as the general trend in the scientific community suggests, it aims at contributing for the spread of this promising technology among particle physics laboratories. It is therefore crucial to foster discussions within the scientific community to promote the development and growth of the innovative idea. As a step toward openness, the best candidate for boosting the finalization of many aspects of the card is the *Open Hardware Repository* (*OHR*, www.ohwr.org). The current manpower devoted to the project is too limited for a prompt coverage and fast reaction time to both the users' specific requirements, and the developer's technology related needs for enhancing the design. The OHR natural inclination toward diversified and parallel developments aiming at a common goal perfectly suits the "needs and wishes" of the A|D|A developers. Profiting from peer review and community based shared developments will bring prompt support, fast feedback, together with a sure visibility of the laboratory's activity.

CONCLUSION AND OUTLOOK

Presently both modules' prototypes (4 boards each) had been successfully tested and debugged, showing performances well within specifications. The A|D|A modules (Figure 16) are in the process of a mini-series production of 20 pieces, expected to be delivered by June. While the A|D|O modules (Figure 17) production will start later this summer. The development of the firmware is continuously growing, including both infrastructural features' improvement and application specific algorithm implementation. Moreover the usage of such cards in other interesting fields of application is being fostered.

Figure 16: A|D|A Prototype Components/Top side

Figure 17: A|D|O Prototype Components/Top side

ACKNOWLEDGMENT

The Author thanks all the Colleagues from the Timing and Diagnostics group at Elettra for the great professional collaboration and the pleasant social company.

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